Preface

The Revision 4 6802 board was not designed by Bob Applegate. It is a continuation of his previous work and is intended to help the hobby community. With Bob's passing it left the only readily available boards for the SS50 Bus being the reproduction SWTPC boards that I make. Where possible I leave the original Corsham manuals intact only making the changes necessary for the upgraded boards. Prior to Bob's passing he had sent me some of his Eagle Design files and library files to help speed the development of my SWTPC replacement motherboard. With Bob's design files it was possible to quickly make reproductions of most of his boards. The continued availability of Corsham's boards gives the hobbyist more choice in building a retro SS50 system.

Frederic Brown

Peripheral Technology
Retired

CORSHAM
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Medford, NJ 08055

6802 CPU Board Rev 4

Introduction

Thank you for buying our 6802 CPU board!

Is this board vintage? Well, it was designed in 2014, so technically it is not. However, it uses a design very similar to the original SWTPC MP-2A using parts available at that time. The large RAM and EPROMs are not vintage, nor are some of the TTL chips.

Using older parts has been a problem because some of them have not been made in a long time, so prices are high, conditions of pulled chips are unknown, and we have to test a lot more components to verify they actually work as expected. Fortunately all the chips on this board are available from surplus inventories, but eventually they will be unavailable.

Features

- 6802 with selectable clock of 1 or 2 MHZ.
- Baud rate generator provides 150, 300, 600, 1200, 2400, 4800, 9600, 19200, or 38400 baud.
- 32K RAM from 0000 to 7FFF.
- RAM from 8000 to EFFF can be enabled/disabled in 4K blocks.
- 8K of ROM from E000 to FFFF; lower 4K can be disabled and/or mapped to RAM.

Summary of Jumpers

There are a number of jumpers on the board that change the behavior. While many of them are discussed in other sections of the manual, here is a summary:

Label	Use
JP4,JP5	JP4 Selects 1MHZ or 2MHZ clock. When JP4 is set to 2MHZ, JP5 can slow the clock to 1MHZ for off board access. When JP4 is a 1MHZ, JP5 has no effect.
JP1 VAR BAUD	Selects which baud rate clock is placed onto the VAR baud rate line. (2400,9600,19200,38400)
JP2 and JP3	Select whether the VAR line is on 110 baud (like 6809 based systems) or 150 baud line (6800).
SW1 RAM ENABLE	An 8 position DIP switch to map the upper 32K of address space to RAM, nothing, or EPROM (only for Exxx).
JP9 RAM ENABLE	Install to enable RAM 0000-7FFF.
JP6,JP7	Select EPROM size and mapping of 8K to 6802: JP6 JP7 EPROM Range 2764 1 1 0000-1FFF 27128 0 1 0000-1FFF 27128 1 1 2000-3FFF 27256 0 0 0000-1FFF 27256 1 0 2000-3FFF 27256 0 1 4000-5FFF 27256 1 1 6000-7FFF

Typical settings for jumpers and switches for 2MHZ system:

Label	Default
JP1 VAR BAUD	9600 baud is common today but any speed can be selected.
JP2 and JP3	JP2 should have the middle and left pins jumpered. JP3 should have the middle and right pins jumpered.
SW1 RAM ENABLE	1 = OFF, 2-6 = ON, 7 = OFF, 8 = ON
JP,JP7	Position 1 - with 2764
JP4,JP8	2MHZ
JP9	Installed - Enable RAM 0000-7FFF

xSWTBUG

We include a version of our extended SWTBUG (xSWTBUG) in EPROM by default. It is fully software compatible with SWTBUG, having all the internal subroutines exactly as they were in the original.

One area of difference is the "C" (clear screen) command has been removed and replaced with the "X" command for extended command set. Using the X command will change the prompt from the normal '$' to '$$' indicating the extended command set. Once in xSWTBUG, there is help available with the '?' command. Exactly which additional features are available in a given version of xSWTBUG depends on the version:

Version 1.1 (initial release)

- M = Memory checker
- O = Othello
- N = Number guess

¡Viva Fiesta!

All of our circuit boards have something unusual on them; and since SWTPC was in San Antonio, it seemed the city would make for some interesting additions. Fortunately, I have a friend who is a native of San Antonio, so I asked her for some ideas or else I'd resort to Googling for something appropriate. She said that ¡Viva Fiesta! is a big festival held in San Antonio each year, so that seemed like a good choice. I was also excited about this board, so the exclamation points fit into my enthusiasm for this project.

Why This?

Back when SWTPC was around, I was a teenager without much money to spare. I got their catalogs and was intrigued by their inexpensive kits and simple designs that could be assembled by average people. The entry point for a working system was a bit beyond my means, so I ended up with a KIM-1 instead.

Years later, I have my own company that has been making Apple/Franklin and KIM-1 expansion boards and one night I decided it was within my abilities to make a clone of the original SWTPC machine. By using some parts available now, the design can be simplified.

Bob Applegate
May 2014

Revision History

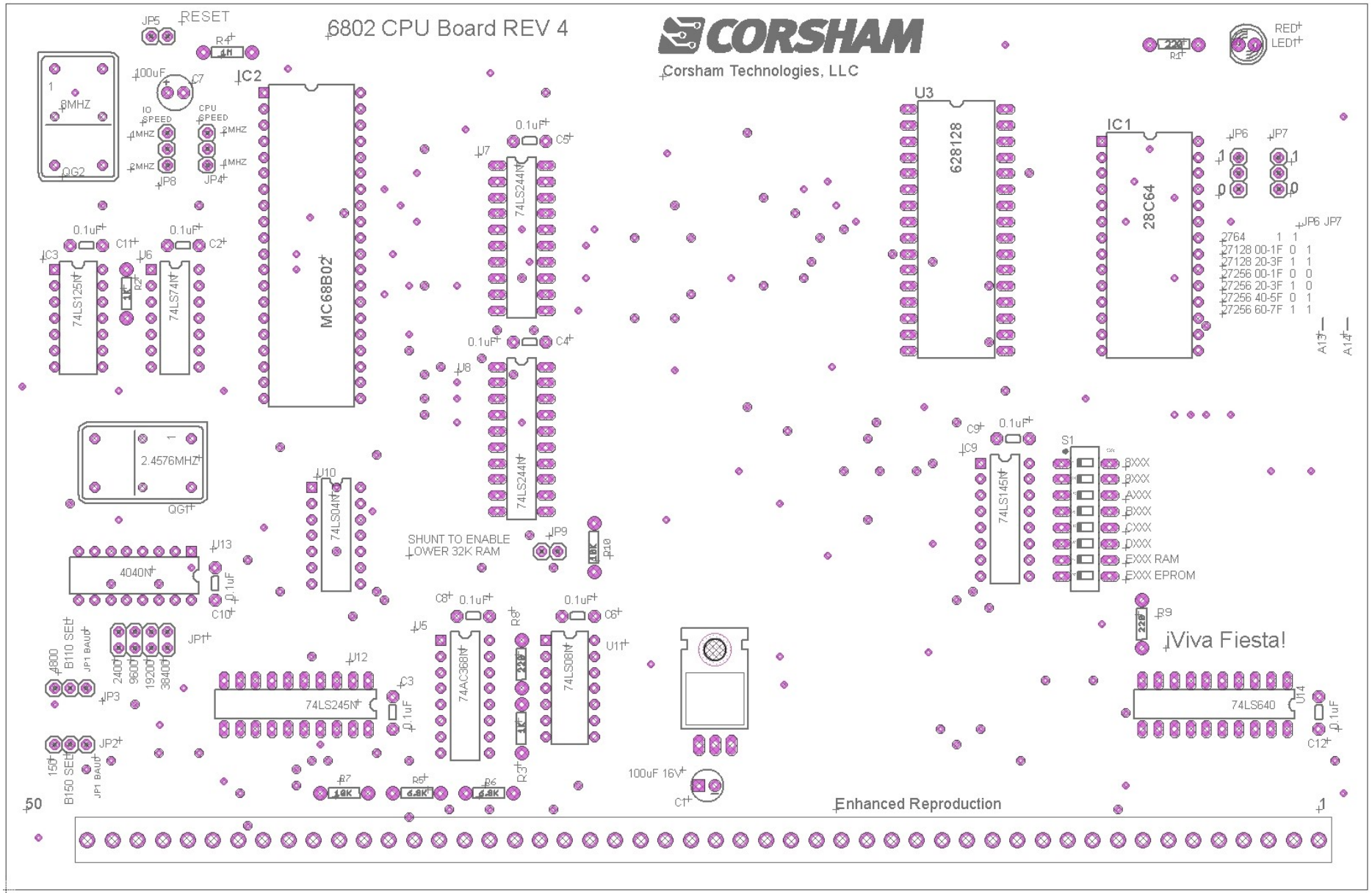
Version	Changes
A	Initial Beta.
1	First official release.
2	Very minor PC board clean-up.
3A	Added a full 60K of RAM. Simplified the baud rate generator.
4	Changed to 6802, added more baud rates, larger EPROM.

Errata

Parts List – Rev 4

Part	Number	Description
PCB	1	Printed Circuit Board
J1	5	Molex 09-52-3101
JP1	1	2x4 jumper block
JP2, JP3,JP4 JP6-JP8	6	1x3 jumper block
S1	1	8 position DIP switch
C1,C7	2	100 uf 16v electrolytic capacitor
C2-C6, C8-C12	10	.1 uf disc capacitor
R1	1	270
R2,R3	1	1K
R4	1	1M
R5, R6	2	6.8K
R7	1	10K
R8, R9	2	220
QD1	1	2.4576 MHz oscillator full size or half size
VR1	1	7805 voltage regulator, TO-220 package
	1	Small Heat Sink and Hardware for 7805
LED1	1	3mm LED
IC1	1	27C64A or 28C64
IC2	1	MC68B02P CPU
U3	1	628128 128K RAM or AS6C1008-55PCN (Digikey)
U5	1	74LS368
U6	1	74LS74
U7,U8	2	74LS244
IC9	1	74LS145

U10	1	74LS04
U11	1	74LS08
U12	1	74LS245
U13	1	CD74HCT4040
U14	1	74LS640
	4	14 pin IC sockets for IC3,U6, U10, U11
	4	16 pin IC sockets for U4, U5, U9, U13
	4	20 pin IC sockets for U7, U8, U12, U14
	1	28 pin IC socket for U2
	1	32 pin IC socket for U3
	1	40 pin IC socket for U1


6802 CPU Board REV 4
CORSHAM
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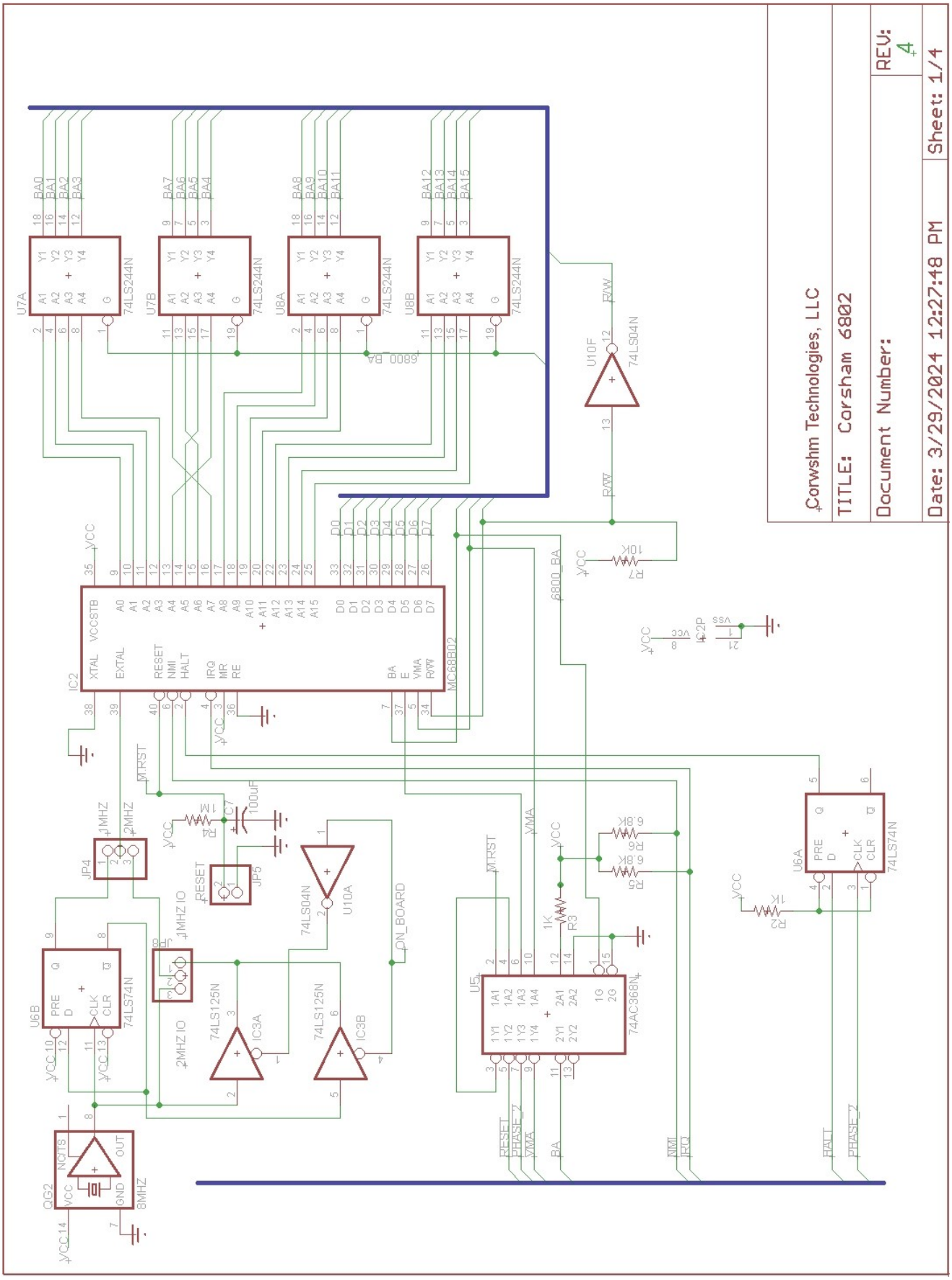
RESET
JP5
R4
4M
100uF
C7
8MHZ
QG2
IO SPEED
CPU SPEED
1MHZ
2MHZ
JP8
JP4
IC2
MC68B02
0.1uF
C3
C11
C2
C5
C4
74LS125N
74LS74N
74LS244N
R2
1K
U6
U7
U8
2.4576MHZ
QG1
U10
74LS04N
SHUNT TO ENABLE LOWER 32K RAM
JP9
R10
10K
4040N
U13
C10
0.1uF
C8
C6
R8
U5
U11
74AC368N
74LS08N
220
1K
R3
JP
4800
9600
19200
38400
B110 SET
JP1 BAUD
JP3
74LS245N
U12
C3
0.1uF
150
B150 SET
JP2
R7
10K
R5
6.8K
R6
6.8K
100uF 16V
C1
U3
628128
IC1
28C64
JP6
JP7
JP6 JP7
2764 1 1
27128 00-1F 0 1
27128 20-3F 1 1
27256 00-1F 0 0
27256 20-3F 1 0
27256 40-5F 0 1
27256 60-7F 1 1
A13
A14
RED LED
220
R1
C9
74LS145N
S1
BXXX
BXXX
AXXX
BXXX
CXXX
DXXX
EXXX RAM
EXXX EPROM
R9
220
¡Viva Fiesta!
74LS640
U14
C12
0.1uF
Enhanced Reproduction
50
1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RESET
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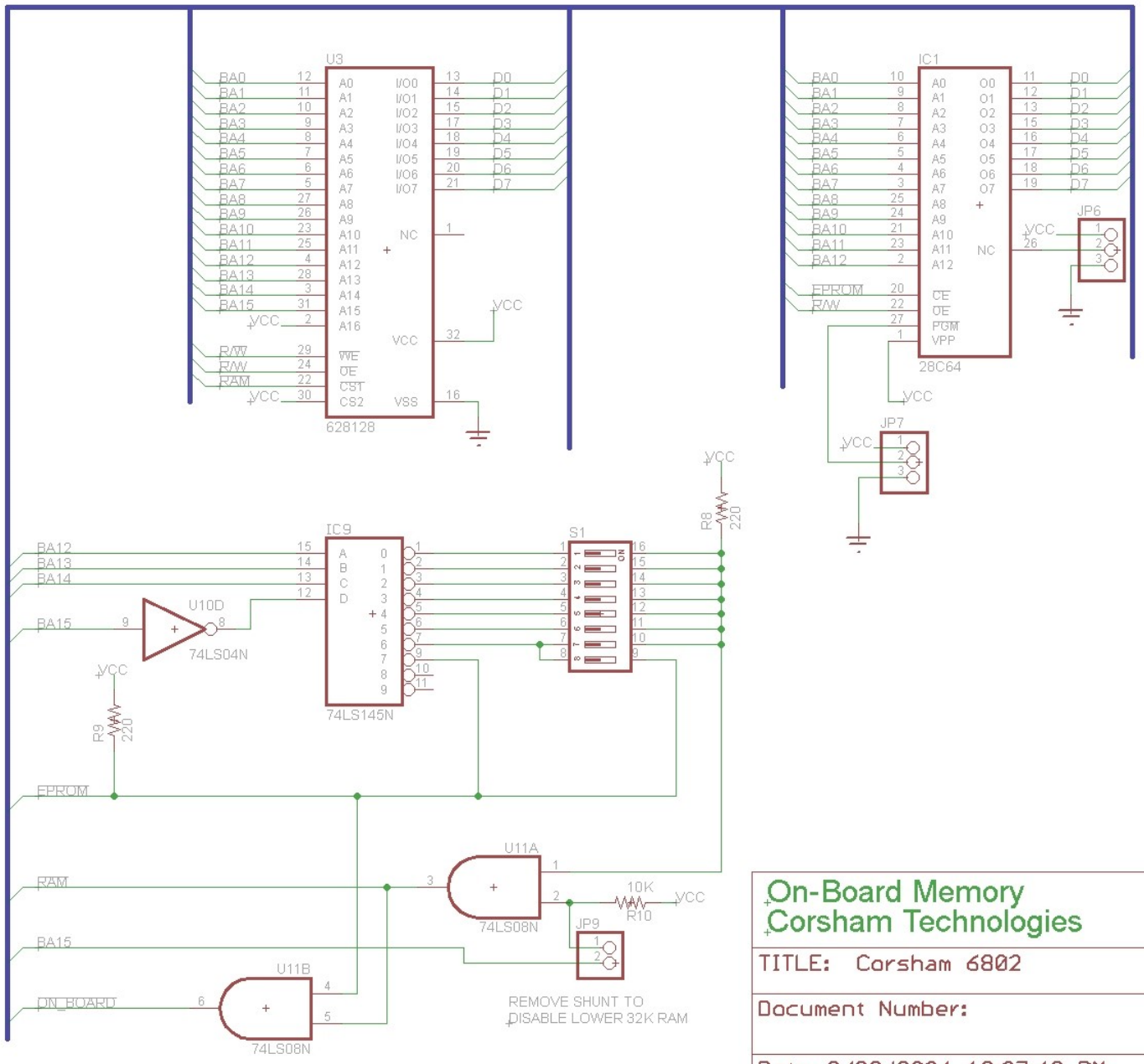
R/W



On-Board Memory
Corsham Technologies

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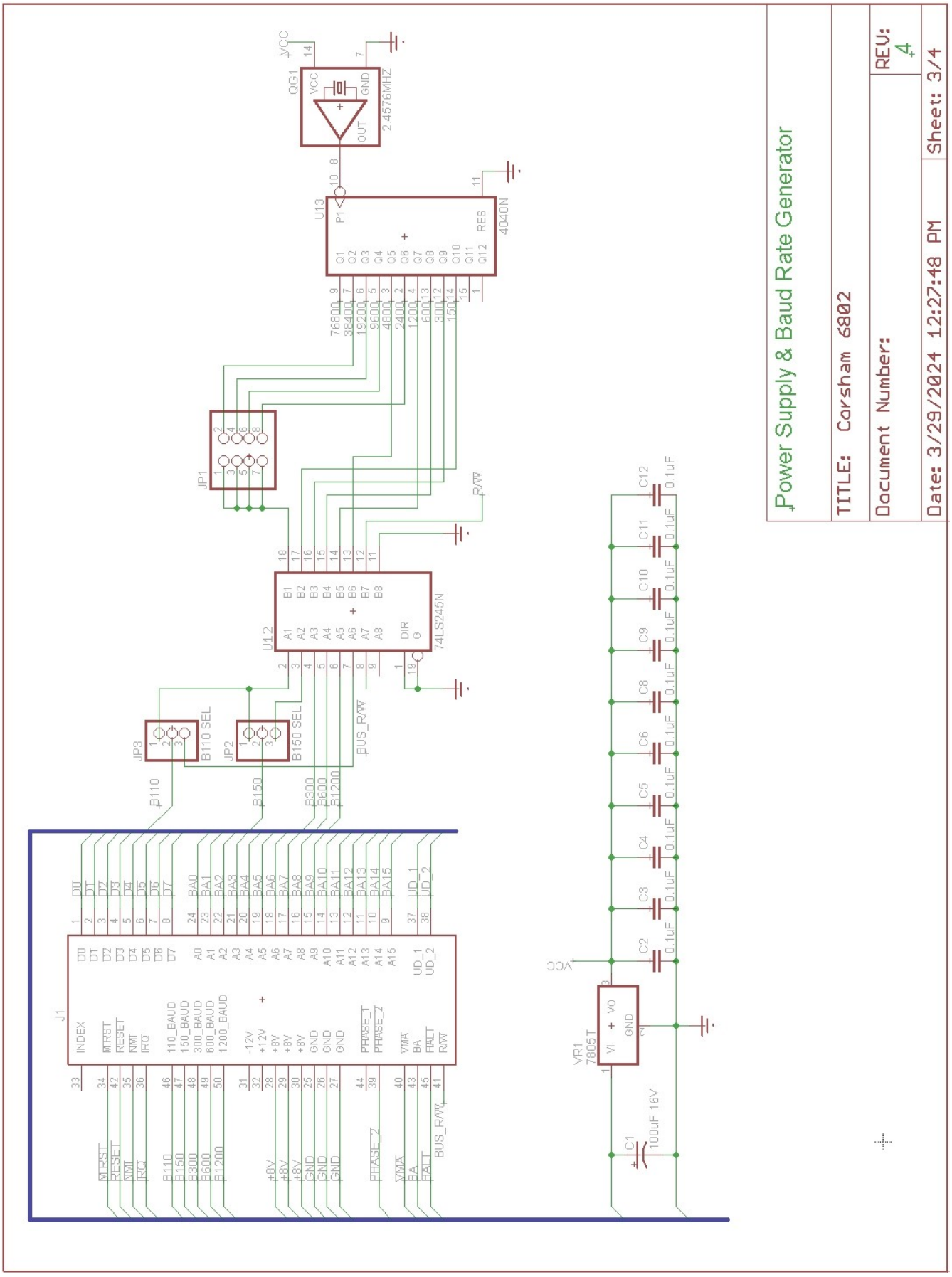
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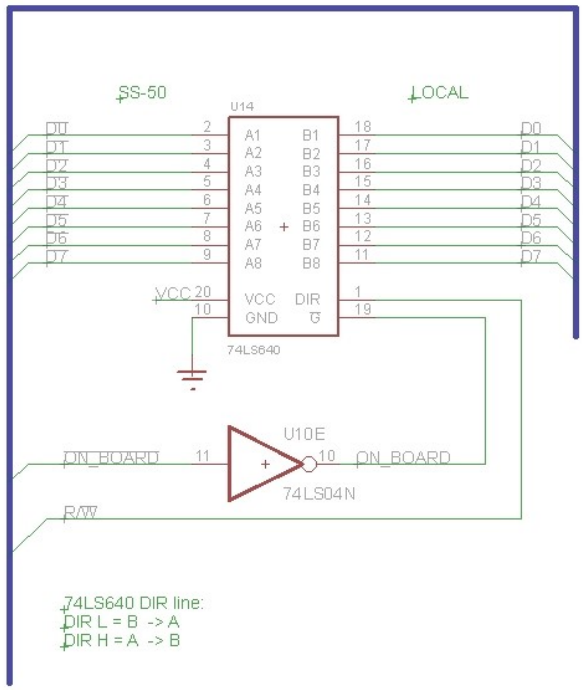
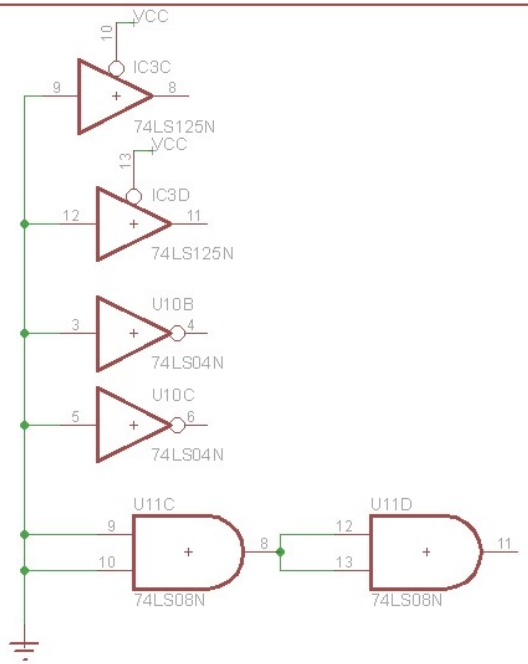
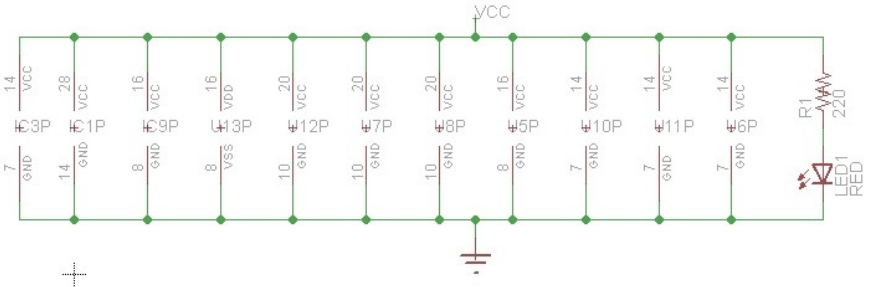
U13
4040N
QG1
24576MHZ
JP1
JP2
JP3
B150 SEL
B110 SEL
VR1
7805T
C1
100uF 16V
0.1uF
BUS_R/W







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