FD-2A

User's Manual

Peripheral Technology
1250 E Piedmont Rd.
Marietta GA 30062

FD - 2A

The FD-2A is a replacement board for the FD2. The FD-2A is slightly smaller and has a solder mask and silkscreen. The FD-2A deletes circuitry that would allow a 1771 floppy controller chip to be used in place of a 2797. The deletion of this build option should not be missed as the option was not described in the user manual. The FD1 controller is available for those who need support of a 1771 controller chip. Other improvements include a ground plane pour to reduce noise on the board. Some hard to find IC's have been replaced with parts that are easier to obtain. Configuring the FD-2A is much simpler. The options can be set by markings on the silkscreen with no need to refer to the user manual. Otherwise the FD-2A works the same as the FD2 it replaces.

The FD-2A is an S-30 size card designed to control up to four drives, single sided/single density to double sided/double density. The FD-2A is compatible with any 6800/6809 S-50 system and can be configured for either four or sixteen addresses per 1/O slot. The FD-2A is both hardware and software compatible with SWTPC DC-1, DC-2, DC-3 and DC-4 type controllers and can use off the shelf versions of Flex with no modifications. Double density operation on a 6800 computer requires a clock frequency of 894 KHZ or greater and new diskette drivers and diskette format program. Both are available as a package from Peripheral Technology. The FD-2A will operate in 2.0 MHZ systems without using any slow I/O circuitry.

Installation

1) If you have purchased the complete system you need only to perform steps 2, 3, 4, 6 and 9. The delivered configuration of the FD-2A is for sixteen addresses per I/O slot and for a 6809 computer.

2) The FD-2A must be configured for either four or sixteen addresses per I/O slot. For SWTPC/6800 and most other 6800 systems this will be four addresses per I/O slot. For SWTPC/6809 with MP-B3 or MP-MB motherboards and most other 6809 systems this will be sixteen addresses per I/O slot.

   **** **IMPORTANT** ****

   On systems that use four addresses per I/O slot, a jumper must be installed on the motherboard. Connect this jumper from I/O select #5 to UDS #3. No jumper is necessary in systems that use sixteen addresses per I/O slot.

3) Install the jumpers for four or sixteen addresses per I/O slot.

(4 addresses)	JP1	Jumper toward 4
	JP2	Jumper toward 4
(16 addresses)	JP1	Jumper toward 16
	JP2	Jumper toward 16

4) On 6800 systems install a jumper JP4 toward 6800.
   On 6809 systems install a jumper JP4 toward 6809.

5) If write precompensation is required remove jumper JP3. You must install a 10K pot at R12. It will require an oscilloscope to set the value. It is unlikely that write precomp will be required. The adjustment is covered in the data separator alignment page.

6) On systems that use four addresses per I/0 slot plug the controller into slot #6.

On systems that use sixteen addresses per I/O slot plug the controller into slot #1.

I/O slots are numbered 0 to 7.

7) Configure the jumpers on your floppy diskette drive(s). If you have bought the complete system this has already been performed. The general requirements for drive configuration are:

(1) Selection of drive select (0, 1, 2, or 3)
(2) Select multiplexed operation
(3) Head should load on drive select.

8. Connect the cable between the controller and the drive(s). Caution: Be certain that pin 1 on the controller connects to pin 1 on the drive(s) or damage may result to both the drives(s) and controller.

9. This completes installation of the FD-2A controller card. Specific system startup instructions are included in the Flex manual. Consult those instructions for booting the system.

Note: The "D" command in the SWTPC monitor (6800) does not reliably boot the system. Use the boot program in the appendix or the one supplied in the Flex manual for reliable boot operation. The "U" bootstrap command in SWTPC's SBUG (6809) monitor does work okay.

Setup and Alignment of The FD-2A Data Separator

Caution: Alignment is performed by Peripheral Technology when the board leaves our factory. Alignment/setup is not required or recommended unless the user changes the WD2797. The user should have technical experience and the use of an oscilloscope. It is not possible to adjust the Data separator by trial and error.

Data Separator

1) Press the computer's reset button.

2) Install a shorting shunt on test jumper JP5.

3) Observe the pulse width on JP6 labeled 1000ns.

4) Adjust R11 for 1000ns pulse width.

5) Observe the frequency on JP6 labeled 125KHZ.

6) Adjust C7 for 125 KHZ

7) Remove the test jumper on JP5.

Write Precompensation

1) Press the computer's reset button.

2) Install a test jumper on JP5.

3) Observe the pulse width on pin 31 of the WD2797.

4) Adjust R12 for desired pulse width (write pre-compensation value)

5) Remove the test jumper on JP5.

FD-2A Jumper Description

JP1,JP2 Sets 4 or 16 addresses per slot. Both jumpers must be set to either 4 or 16

JP3 Shorted - No write precompensation
Open - write pre-compensation, amount determined by adjustment of R12.

JP4 Source of ready signal of WD2797
for 4 addresses per I/O slot set to 6800
for 16 addresses per I/O slot set to 6809

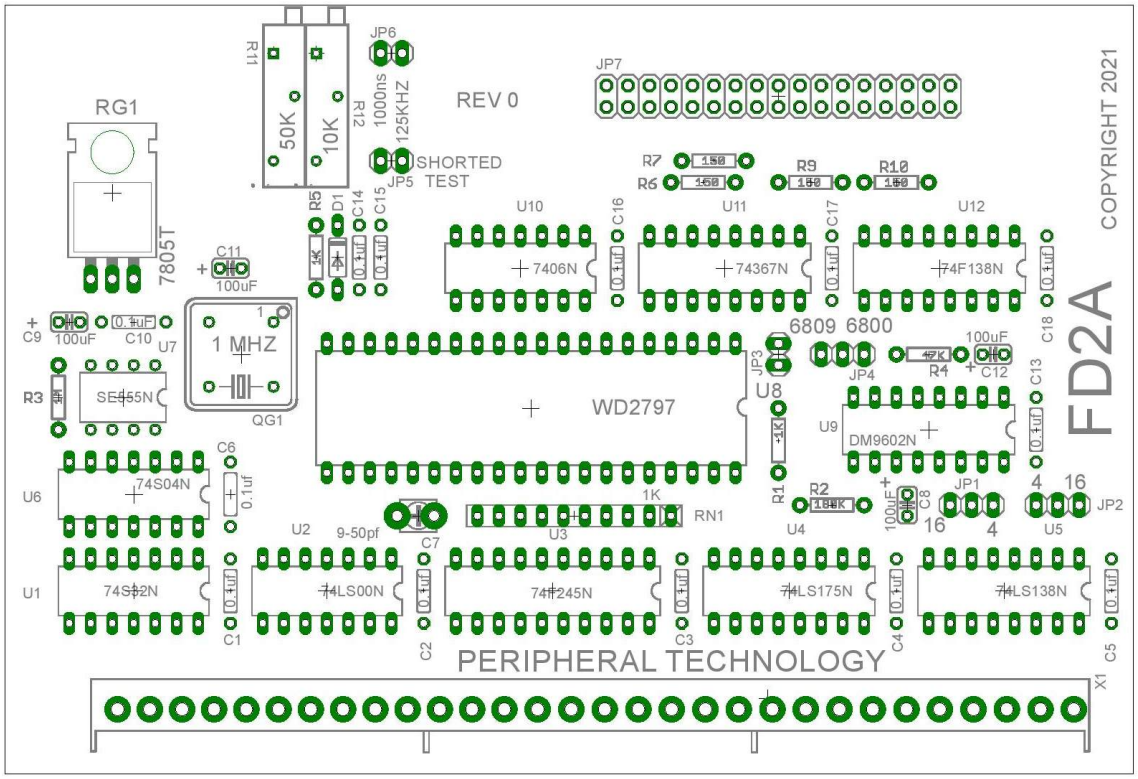
JP5 Test Jumper - Shorted to adjust data separator
Note - Board will not function if test jumper is not removed after adjustment.

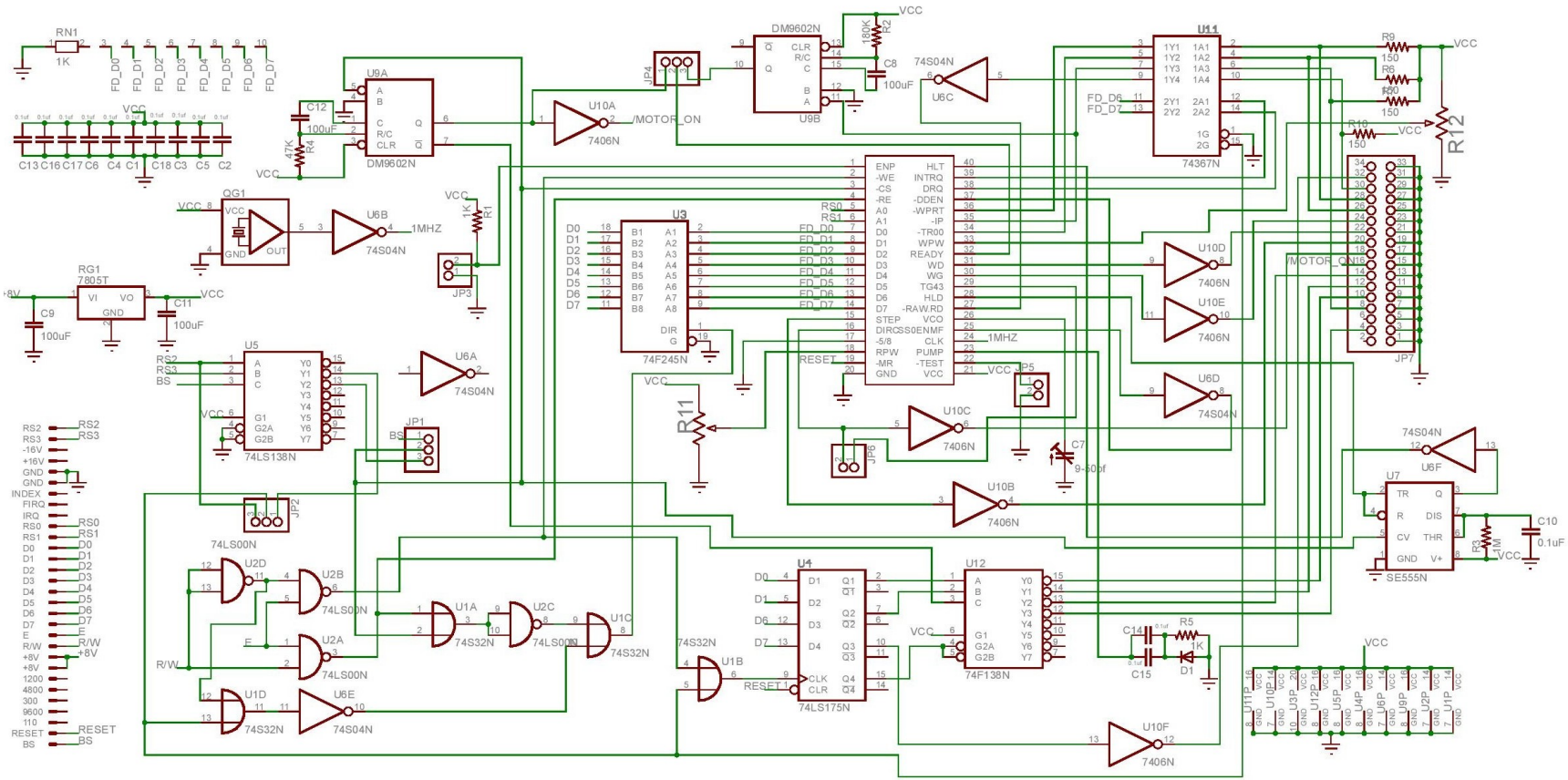
JP6 A test point to attach an oscilloscope or frequency counter when adjusting the data separator.

Parts List FD-2A

Quantity	Designation	Description
2	R1,R5	1K 1/4 Watt Resistor
1	R2	180K 1/4 Watt Resistor
1	R3	1M 1/4 Watt Resistor
1	R4	47K 1/4 Watt Resistor
1	R2	180K 1/4 Watt Resistor
4	R6,R7,R9,R10	150 1/4 Watt Resistor
1	R11	50K 18 turn Pot
1	R12	10K 18 turn Pot - Optional - only for write precompensation
1	RN1	1K 10 Pin Sip Resistor
12	C1-C6,C10	
	C13-C18	0.1 uf Disc Cap
1	C7	9-50 pf Variable Capacitor
4	C8,C9,C11,C12	100 uf 16V Electrolytic Capacitor
1	U1	74LS32
1	U2	74LS00
1	U3	74F245
1	U4	74LS175
1	U5	74LS138
1	IC6	74LS04
2	U7	555
1	U8	WD2797
1	U9	DM9602N
1	U10	7406
1	U11	74LS367
1	U12	74F138 Not Critical 74LS138 OK
1	RG11	7805
1	D1	1N4148
1	QG1	1.0 MHZ Oscillator half size
1		17x2 male header
3		10 pin female molex socket
1		8 Pin IC Socket
4		14 Pin IC Socket
5		16 Pin IC Socket
1		20 Pin IC Socket
1		40 Pin IC Socket
3		3x1 pin header strip
3		2x1 pin header strip
4		Shorting Plugs
1		Heat sink
1		6-32 x 3/8 screw
1		#6 Washer
1		6-32 Nut
1		Index Pin for Molex Connector
1		FD-2A Board

Parts Placement FD-2A




RN1
1K
FD_D0
FD_D1
FD_D2
FD_D3
FD_D4
FD_D5
FD_D6
FD_D7
VCC
C13 C16 C17 C6 C4 C1 C18 C3 C5 C2
U9A
C12
100uF
R4
47K
DM9602N
U10A
7406N
/MOTOR_ON
JP4
DM9602N
U9B
180K
R2
C8
100uF
74S04N
U6C
U11
74367N
FD_D6
FD_D7
R9
150
R8
150
R10
150
R12
OG1
U6B
1MHZ
74S04N
R1
1K
JP3
RG1
7805T
C9
100uF
C11
100uF
U3
74F245N
D0
D1
D2
D3
D4
D5
D6
D7
RS0
RS1
FD_D0
FD_D1
FD_D2
FD_D3
FD_D4
FD_D5
FD_D6
FD_D7
1MHZ
RESET
JP5
U10D
7406N
U10E
7406N
U6D
74S04N
U10C
7406N
JP6
C7
9-50pf
U10B
7406N
U5
74LS138N
RS2
RS3
BS
U6A
74S04N
JP1
JP2
74LS00N
U2D
U2B
U2A
U1A
U2C
U1C
74S32N
74LS00N
74S32N
R/W
U1D
U6E
74S04N
U4
74LS175N
U1B
74S32N
RESET
U12
74F138N
C14
C15
R5
1K
D1
U10F
7406N
74S04N
U6F
U7
SE555N
R3
1M
C10
0.1uF
INDEX
FIRQ
IRQ
-16V
+16V
+8V
1200
4800
300
9600
110
BS

```
    2                           OPT     PAGE

BOOT                                    7-17-83  TSC ASSEMBLER  PAGE    1

    4                   * THIS PROGRAM IS USED TO BOOT FLEX WITH A FD-1 OR
    5                   * FD-2 CONTROLLER CARD
    6                   *
    7                   * COPYRIGHTED 1983 BY PERIPHERAL TECHNOLOGY
    8                   *
    9  8014             DRVREG  EQU     $8014
   10  8018             COMREG  EQU     $8018
   11  801A             SECREG  EQU     $801A
   12  801B             DATREG  EQU     $801B

   14  0100                     ORG     $0100

   16  0100 4F          START   CLR A            SELECT DRIVE 0
   17  0101 B7 80 14            STA A   DRVREG    WRITE TO DRIVE SELECT REGISTER
   18  0104 B6 80 18            LDA A   COMREG    READ COMREG TO ALLOW MOTOR TO START
   19  0107 CE FF FF            LDX     ##$FFFF   WAIT FOR MOTOR TO START
   20  010A 01          WAIT    NOP               "
   21  010B 01                  NOP               "
   22  010C 09                  DEX               "
   23  010D 26 FB               BNE     WAIT      "
   24  010F 86 0B               LDA A   ##$0B     ISSUE RESTORE COMMAND
   25  0111 B7 80 18            STA A   COMREG    "
   26  0114 8D 2A               BSR     DELAY     WAIT BEFORE READING STATUS REGISTER
   27  0116 F6 80 18  WAIT1     LDA B   COMREG    WAIT FOR RESTORE TO COMPLETE
   28  0119 C4 01               AND B   #1        "
   29  011B 26 F9               BNE     WAIT1     "
   30  011D 7F 80 1A            CLR     SECREG    SET SECTOR REGISTER TO 0
   31  0120 86 9C               LDA A   ##$9C     READ SECTOR COMMAND
   32  0122 B7 80 18            STA A   COMREG    EXECUTE READ COMMAND
   33  0125 8D 19               BSR     DELAY     WAIT BEFORE READING STATUS REGISTER
   34  0127 CE 24 00            LDX     ##$2400   LOAD ADDRESS
   35  012A B6 80 18  READ      LDA A   COMREG    READ STATUS REGISTER
   36  012D 85 02               BIT A   #2        CHECK FOR DRQ
   37  012F 26 07               BNE     READ1     YES = READ DATA
   38  0131 85 01               BIT A   #1        CHECK FOR BUSY
   39  0133 26 F5               BNE     READ      YES = REPEAT LOOP
   40  0135 7E 24 00            JMP     $2400     EXECUTE LOADED PROGRAM
   41  0138 B6 80 1B  READ1     LDA A   DATREG    GET DATA
   42  013B A7 00               STA A   X         STORE IT
   43  013D 08                  INX               BUMP LOAD POINTER TO NEXT LOCATION
   44  013E 20 EA               BRA     READ      GET NEXT BYTE
   45  0140 8D 00       DELAY   BSR     DELAY1    DELAY ROUTINE
   46  0142 8D 00       DELAY1  BSR     DELAY2
   47  0144 39          DELAY2  RTS
   48                           END

NO ERROR(S) DETECTED
```