PT-XTIDE

User's Manual

Peripheral Technology

Last update 05/08/26

PT-XT-IDE

The XT-IDE is a modern replacement for an IDE controller Peripheral Technology sold in the 80's. That controller is no longer available and doesn't work well with modern drives utilizing LBA addressing. There are two versions of the board - one is for the PT68K2 or PT68K4 and the other is for the PT68K5. The only difference between the boards is the speed of the GAL used.

In the PT68K2/4 computer, the XT-IDE will be the main controller board. In the PT68K5, the XT-IDE is usually a second controller since the PT68K5 has a built in IDE port that is far faster than the XT-IDE board.

There are versions of OS9, SK*DOS and REX that support this board.

Parts List XT-IDE

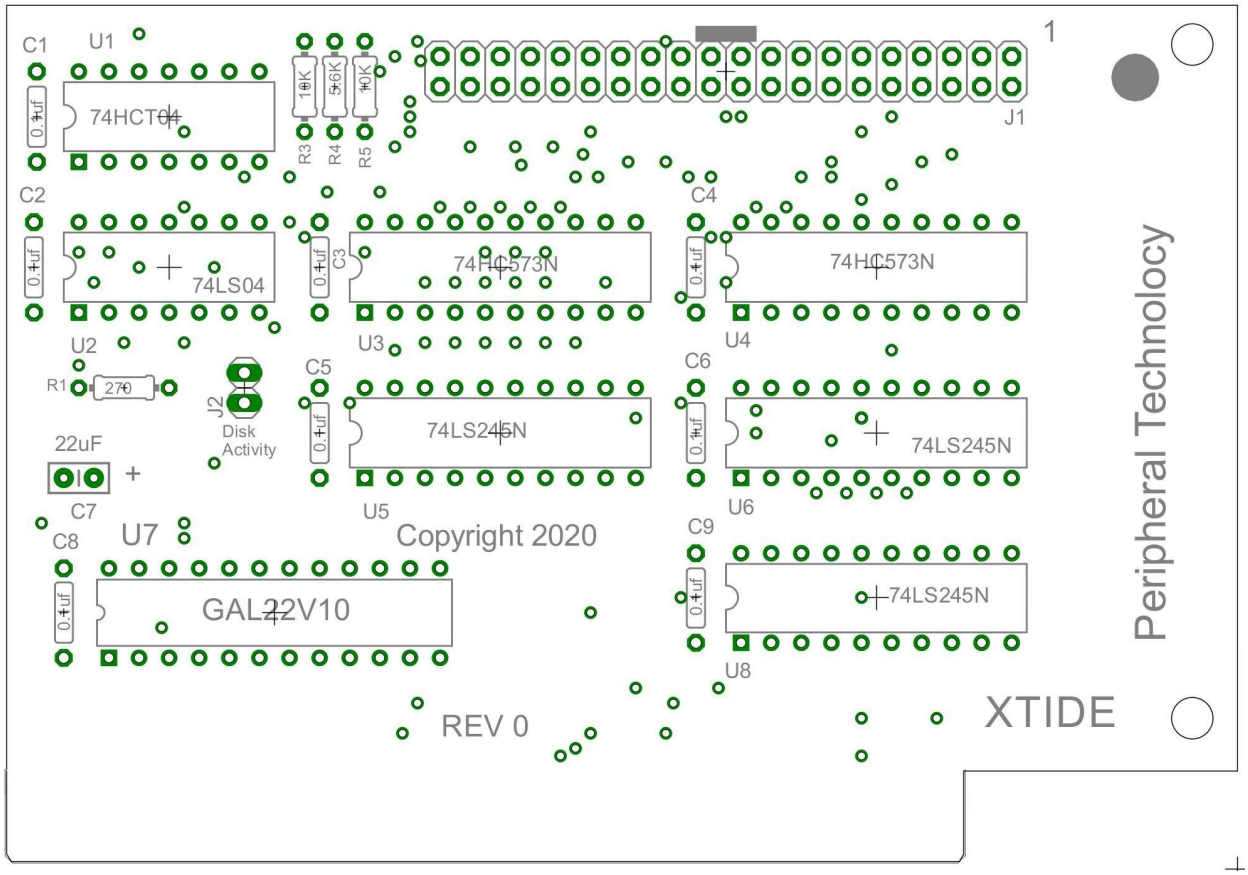
Quantity	Designation	Description
1	R1	270 Ohm 1/4 Watt Resistor
2	R3,R5	10K Ohm 1/4 Watt Resistor
1	R4	5600 Ohm ¼ Watt resistor
8	C1-C6,C8,C9	0.1uF Ceramic Capacitor
1	C7	20 to 100uF 16V Capacitor
1	U1	74HCT04
1	U2	74LS04
2	U3-U4	74HCT573
3	U5,U6,U8	74HCT245
1	U7	Atmel F22V10C-10PU for PT68K5 Atmel F22LV10CQZ-30PU PT68K2 or 4
2		14 pin IC Socket
5		20 pin IC Socket
1		24 pin IC Socket .3” width
1	J1	20x2 Header Strip
1	J2	2x1 Header Strip – or generic LED
1		Keystone 9202 Bracket

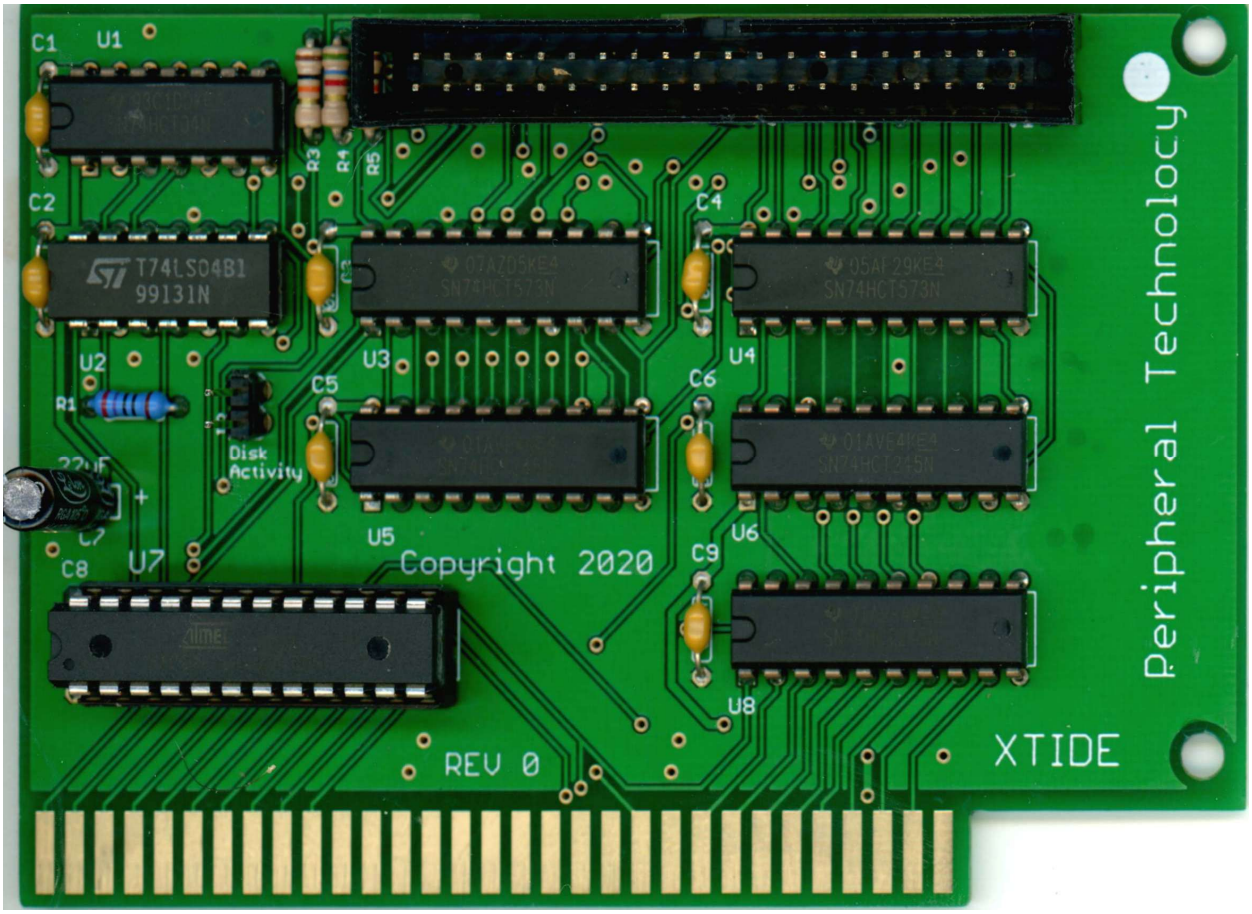
Notes:
Speed of the 22V10s is critical; don’t substitute different speed parts. Only Atmel brand parts have been tested.

J2 can either have a header for an external LED or an LED may be installed in J2.

The silkscreen on the board shows the wrong type of ICs - for instance 74LS245 when the part is 74HCT245. Please use the parts list and not the silkscreen.

Parts Placement PT-XT-IDE

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U1
R3
R4
R5
C2
T74LS04B1
99131N
U2
R1
Disk
Activity
C7
C8
U7
C3
U3
C5
U5
C4
U4
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U6
C9
U8
Copyright 2020
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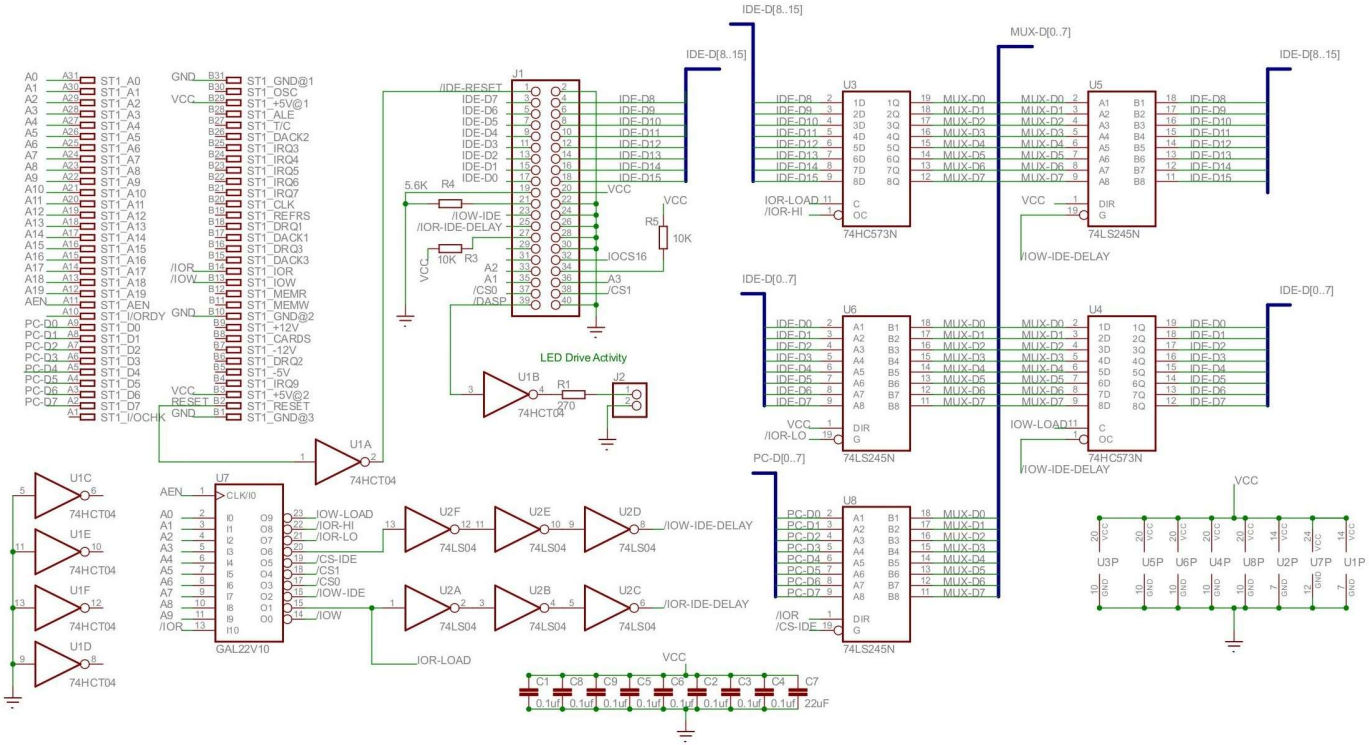

TITLE: XTIDE	
Document Number:	REV:
Date: 5/8/2026 2:35:13 PM	Sheet: 1/1

U7 PAL Equations

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Name     PTIDE8 ;
PartNo   U7 ;
Date     9/27/2020 ;
Revision 00 ;
Designer Frederic Brown ;
Company  Peripheral Technology ;
Assembly None ;
Location  ;
Device   g22v10 ;

/* *************** INPUT PINS *********************/
PIN  1   =   AEN                    ; /*                                 */
PIN  2   =   A0                     ; /*                                 */
PIN  3   =   A1                     ; /*                                 */
PIN  4   =   A2                     ; /*                                 */
PIN  5   =   A3                     ; /*                                 */
PIN  6   =   A4                     ; /*                                 */
PIN  7   =   A5                     ; /*                                 */
PIN  8   =   A6                     ; /*                                 */
PIN  9   =   A7                     ; /*                                 */
PIN  10  =   A8                     ; /*                                 */
PIN  11  =   A9                     ; /*                                 */
PIN  12  =   GND                    ; /*                                 */
PIN  13  =   !IOR                   ; /*                                 */
PIN  14  =   !IOW                   ; /*                                 */
pin  24  =   Vcc                  ; /*                               */

/* *************** OUTPUT PINS *********************/
PIN  15  = IOR_LOAD                 ; /*                                 */
PIN  16  = !IOW_IDE                 ; /*                                 */
PIN  17  = !CS0                     ; /*                                 */
PIN  18  = !CS1                     ; /*                                 */
PIN  19  = !CS_IDE                  ; /*                                 */
PIN  20  = !IOW_IDE_DELAY           ; /*                                 */
PIN  21  = !IOR_LO                  ; /*                                 */
PIN  22  = !IOR_HI                  ; /*                                 */
PIN  23  = IOW_LOAD                 ; /*                                 */



CS_IDE = !A5 & !A6 & !A7 & A8 & A9  ;


CS0 =   !A4 & !A5 & !A6 & !A7 & A8 & A9  ;


CS1 =  A4 & !A5 & !A6 & !A7 & A8 & A9  ;

IOW_IDE =  !(!A0 & !A1 & !A2 & !A3) & !A5 & !A5 & !A6 & !A7 & A8 & A9 & IOW  ;


!IOW_IDE_DELAY = !(!A0 & !A1 & !A2 & !A3) & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW   ;


IOR_HI =   A0 & !A1 & !A2 & !A3 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR ;
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```
IOR_LO =     !A3 & !A2 & !A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 & !A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 & !A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 &  A2 & !A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 &  A2 & !A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 &  A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 &  A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 & !A2 & !A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 & !A2 & !A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 & !A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 & !A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 &  A2 & !A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 &  A2 & !A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 &  A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 &  A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR

 ;

IOW_LOAD = (!A0 & !A1 & !A2 & !A3 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW  )

        #    (!A3 & !A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    (!A3 & !A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    (!A3 &  A2 & !A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    (!A3 &  A2 & !A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    (!A3 &  A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    (!A3 &  A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    ( A3 & !A2 & !A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    ( A3 & !A2 & !A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    ( A3 & !A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    ( A3 & !A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    ( A3 &  A2 & !A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    ( A3 &  A2 & !A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    ( A3 &  A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )
        #    ( A3 &  A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOW )  ;


IOR_LOAD =   !A3 & !A2 & !A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 & !A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 & !A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 &  A2 & !A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 &  A2 & !A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 &  A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #    !A3 &  A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 & !A2 & !A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 & !A2 & !A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 & !A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 & !A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 &  A2 & !A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 &  A2 & !A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 &  A2 &  A1 & !A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR
        #     A3 &  A2 &  A1 &  A0 & !A4 & !A5 & !A6 & !A7 & A8 & A9 & IOR  ;
```