Altair 680

MIO

User's Manual

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Introduction

The Peripheral Technology MIO (Memory/IO) board is designed to replace MITS memory and UIO boards. The MIO provides up to 60K RAM and up to 32k of EPROM. RAM and EPROM can be enabled in 4k blocks. The MIO board decodes memory in the top 4K of EPROM from F100-FFFF. The addresses between F000-F0FF are used for IO in the Altair. EPROM on the MIO can replace the 1702s on the main board. It's as simple as removing the 1702s on the main board and enabling EPROM in the F100-FFFF range using the MIO configuration switches. The first 1K of RAM on the MIO can be disabled so no changes are required on the main board, and the 1K on the main board does not conflict with the RAM on the MIO. The MIO provides two parallel ports, a serial port, real time clock, and two IDE channels. The parallel ports are compatible with the UIO board with 24 pin sockets as was provided on the UIO. Assembled MIO boards ship with an SWTBUG monitor ROM. SWTBUG can boot FLEX from the IDE ports, serial FLEX from Mike Douglas, and FLEX from the Corsham sd card system. An adapter is available for the Corsham system so no custom cables are necessary. The assembled board includes an SD card, preloaded with FLEX, an SD to IDE adapter and a cable. The Altair front panel can read and write to the MIO RAM.

MIO MEMORY MAP

```
0000-EFFF RAM           ENABLED IN 4K BLOCKS
8000-EFFF EPROM         ENABLED IN 4K BLOBKS
F100-FFFF EPROM         ADDRESSES F000-F0FF NOT AVALABLE SINCE THEY CONFLICTS WITH IO

F006-F007 MC6850 ACIA   ASSUMES BASE ADDRESS OF F006-F00F
F008-F00B MC6821 PIA    ASSUMES BASE ADDRESS OF F006-F00F
F00C-F00F MC6821 PIA    ASSUMES BASE ADDRESS OF F006-F00F
F0C0-F0CF MC146818 RTC
F0D0-F0DF IDE 0
F0E0-F0EF IDE 1
```

The address of the ACIA and PIAs assume the MIO is configured for addresses F006-F00F. The MIO can be configured to start on 16-byte intervals from F000 to F0B0. The first six bytes are not decoded or used since they would conflict with the main board.

MC6821 PIA

The PIA ports are provided with 24 pin dip sockets as well as a 50-pin dual header strip commonly used in other Peripheral Technology products. The 24 pin socket uses the same pinout as the MITS UIO board. MITS inverted address line A0 to the MC6821 which changed the arrangement of the registers. There is a jumper on the MIO so you can keep the MITS standard or use a non-inverted A0 to the MC6821 like most everyone else does. This provides choice and allows software written for the MITS UIO board to be used unchanged, or if you are bringing programs from other sources you don't have to modify your program.

MC6850 ACIA RS232

The MC6850 provides a serial port. Baud rates are selectable by jumper. Available baud rates are 300, 1200, 9600, 19200, 38400 and 57600. A DB9F is located at the rear corner of the MIO and is wired so common DB9M to USB serial adapter cables are a direct plug in.

RAM

Up to 60k of RAM is selectable by a dip switch in 4k blocks starting at address 0000. There is a jumper to disable the first 1k of RAM at address 0000-03FF so that it is not necessary to modify the main board when using the MIO board. The main board would typically have 1K of RAM at address 0000. The RAM chip used is a 128Kx8. Only half of the chip is used. The selection of a 128Kx8 chip was because 64Kx8 RAM chips are extremely rare.

EPROM

Up to 32k of EPROM is selectable by a dip switch. EPROM is selectable in 4k blocks starting at address 8000. The address decoding on the MIO does not decode addresses F000-F0FF. These addresses are reserved for IO use on the Altair 680. The EPROM on the MIO can be used to replace the 1702s of the main board. No modifications are necessary to the main board. Just remove all of the 1702s and select the F000-FFFF EPROM memory block using dip switch S1. When enabling EPROM be sure that RAM is not selected at the same address. A 27512 EPROM is used and there is a jumper to select either the upper or lower half of the EPROM. This allows two separate monitors to be selected by a jumper on the MIO board. A 27512 is a 64K EPROM. When the lower/upper jumper is in lower, the first 32K of the EPROM is mapped to address 8000-FFFF of the processor. When the jumper is set to upper, EPROM addresses 8000-FFFF are mapped to processor addresses 8000-FFFF. Selectable in 4K blocks.

MC146818 Real Time Clock

The real time clock chip will supply the date to FLEX on powerup for the version of FLEX that boots on the IDE. There is a battery holder on the MIO to power the clock chip when power is switched off to the Altair 680. The battery used is a CR123a lithium battery. This battery can be obtained at places like Home Depot, Lowes, some grocery stores, and online. The MC146818 can be programmed to generate a source of interrupts for real time applications.

IDE Ports

There are two IDE ports. Currently IDE0 is used to boot FLEX. IDE1 is used by a FLEX utility to backup or restore partitions to an SD card using IDE1. Assembled MIO boards ship with FLEX preloaded on an SD card.

SWTBUG Monitor

Assembled MIO boards ship with an enhanced SWTBUG monitor installed. This is a greatly improved version of the SWTBUG that SWTPC supplied. There is a dedicated manual for SWTBUG, and SWTBUG will not be covered here except to list the commands.

```
A               - DISASSEMBLE FROM MEMORY
B XXXX          - SET BREAKPOINT AT ADDRESS XXXX
C               - CLEAR SWTPC CT-1024 TERMINAL SCREEN
D               - BOOT DISK - LOADS FROM SECTOR 0
E               - PUNCH END OF TAPE CODE
F YYYY XXXX ZZ  - FIND BYTE ZZ FROM ADDRESS XXXX TO ADDRESS YYYY
G               - EXECUTE PROGRAM FROM ADDRESS STORED AT A048-A049
J XXXX          - EXECUTE PROGRAM AT ADDRESS XXXX
H               - REENTER FLEX - JUMP TO ADDRESS AD03
I XXXXX YYYY ZZ - SET MEMORY FROM XXXX TO YYYY WITH ZZ
L               - LOAD S RECORDS
M XXXX          - MEMORY EXAMINE/CHANGE
O               - OPTIONAL PORT COMMAND
P               - PRINT S RECORD FROM ADDRESS STORED AT A002-A005
Q XXXX YYYY     - TEST MEMORY FROM XXXX TO YYYY
R               - REGISTER DUMP
T               - TRACE COMMAND
U               - BOOT FLOPPY - LOAD FROM SECTOR 1
V XXXX YYYY     - VIEW HEX/ASCII FROM ADDRESS XXXX TO YYYY
W               - BOOT FROM IDE CONTROLLER
```

ALTAIR 680 COMMANDS

```
S            - BOOT SERIAL FLEX
X            - BOOT CORSHAM SD CARD SYSTEM AND UTILITIES
Z            - JUMP TO ALTAIR MONITOR

NOTE: THE O COMMAND DOES NOT FUNCTION ON THE ALTAIR.
```

Jumper Options

JP1 1 – R/W from Bus is Buffered
2 – R/W from Bus is passed to MIO board

JP2 1 – PHI2 from Bus is Buffered
2 - PHI2 from Bus is passed to MIO board

JP3 Baud Rates – Only install one jumper. Baud rate selections are 300, 1200, 9600, 19200, 38400 and 57400.

JP4 DCD enable. Jumper connects Pin 4 from the DB9F to control the DCD line on the MC6850. If not shorted there is a pull up resistor that forces DCD to always be enabled.

JP5 CTS Enable. Position 1 forces CTS on. Position 2 allows pin 7 of the DB9F to control the CTS pin on the MC6850.

JP6 EPROM Select – Lower or Upper. This jumper selects either the Lower or Upper half of a 27512 EPROM. This allows for two separate monitor programs to be selected by changing the jumper.

JP7 1K RAM Disable – OPEN – Use RAM from 0000-03FF on the main board.
Shorted – Use RAM from 0000-03FF on the MIO board.
If JP7 is shorted you must modify the main board so the RAM on the main board does not conflict with the RAM on the MIO board.

JP8 Enable IRQ from MC146818. The MC146818 sometimes generates an IRQ on powerup. Unless the IRQ is cleared by software, the system can hang when IRQs are enabled. This jumper should not be enabled unless your software deals with the power up IRQ.

JP9 A0 selection to MC6821s:
Position 1 – A0 Inverted
Position 2 – A0 Not inverted
MITS inverted A0 on their UIO board. This causes the data and control registers to be reversed. For compatibility with the UIO board select Position 1. If you have no need for compatibility with the UIO board it might be easier to use Position 2. This would allow software from other sources to be used without the need to modify the register definitions. Position 1 should be used if you plan to use the Corsham SD card system.

JP10 MC6821 Parallel Port: JP10 and J3 are connected in parallel and only one should be used. JP10 uses a 50-pin header with the same connections as other Peripheral Technology boards. Assuming the MIO is configured as board 0 – the address of this PIA is F00C-F00F.

J3 24 Pin Dip socket. Wired the same as the MITS UIO board J3 connector.

JP11 Shorted - Feed +5V to pins 7 and 8 of J3.

JP12 Shorted – Feed +5V to pin 9 on the DB9F – Intended for a power source to an EPS32 file server used with serial FLEX.

JP13 MC6821 Parallel Port: JP13 and J4 are connected in parallel and only one should be used. JP10 uses a 50-pin header with the same connections as other Peripheral Technology boards. Assuming the MIO is configured as board 0 – the address of this PIA is F008-F00B.

J4 24 Pin Dip socket. Wired the same as the MITS UIO board J4 connector.

JP14 Shorted – Feed +5V to pins 7 and 8 of J4

JP15 IDE 1

JP16 IDE 0

JP17 Clock Out from MC146818

SWITCH SETTINGS

Switches S1, S2 and S3 configure the MIO on board RAM and EPROM. RAM and EPROM can be selected in 4K block boundaries. You should not configure RAM and EPROM for the same address.

Switch S1 – EPROM

Dip Switch S1 – Enables EPROM. There are 8 switches and they enable EPROM in 4K block sizes from 8000-FFFF. The address being enabled is shown on the MIO silkscreen to the right of S2. Setting the switch to the ON position enables the block.

S1 – 1 F100-FFFF – Memory from F000-F0FF is not enabled since memory in this range is used for IO.
S1 – 2 E000-EFFF
S1 – 3 D000-DFFF
S1 – 4 C000-CFFF
S1 – 5 B000-BFFF
S1 – 6 A000-AFFF
S1 – 7 9000-9FFF
S1 – 8 8000-8FFF

Switch S2 and S3 – RAM

Switch S2 and S3 enables RAM. Setting the switch to the ON position enables RAM.

S2 – 1 F100-FFFF
S2 – 2 E000-EFFF
S2 – 3 D000-DFFF
S2 – 4 C000-CFFF
S2 – 5 B000-BFFF
S2 – 6 A000-AFFF
S2 – 7 9000-9FFF
S2 – 8 8000-8FFF

S3 – 1 7000-7FFF
S3 – 2 6000-6FFF
S3 – 3 5000-5FFF
S3 – 4 4000-4FFF
S3 – 5 3000-3FFF
S3 – 6 2000-2FFF
S3 – 7 1000-1FFF
S3 – 8 0000-0FFF

Note: If JP7 is open S3-8 will enable RAM from 0400-0FFF.

Switch S4 – Base Address of 6850 and 6821s

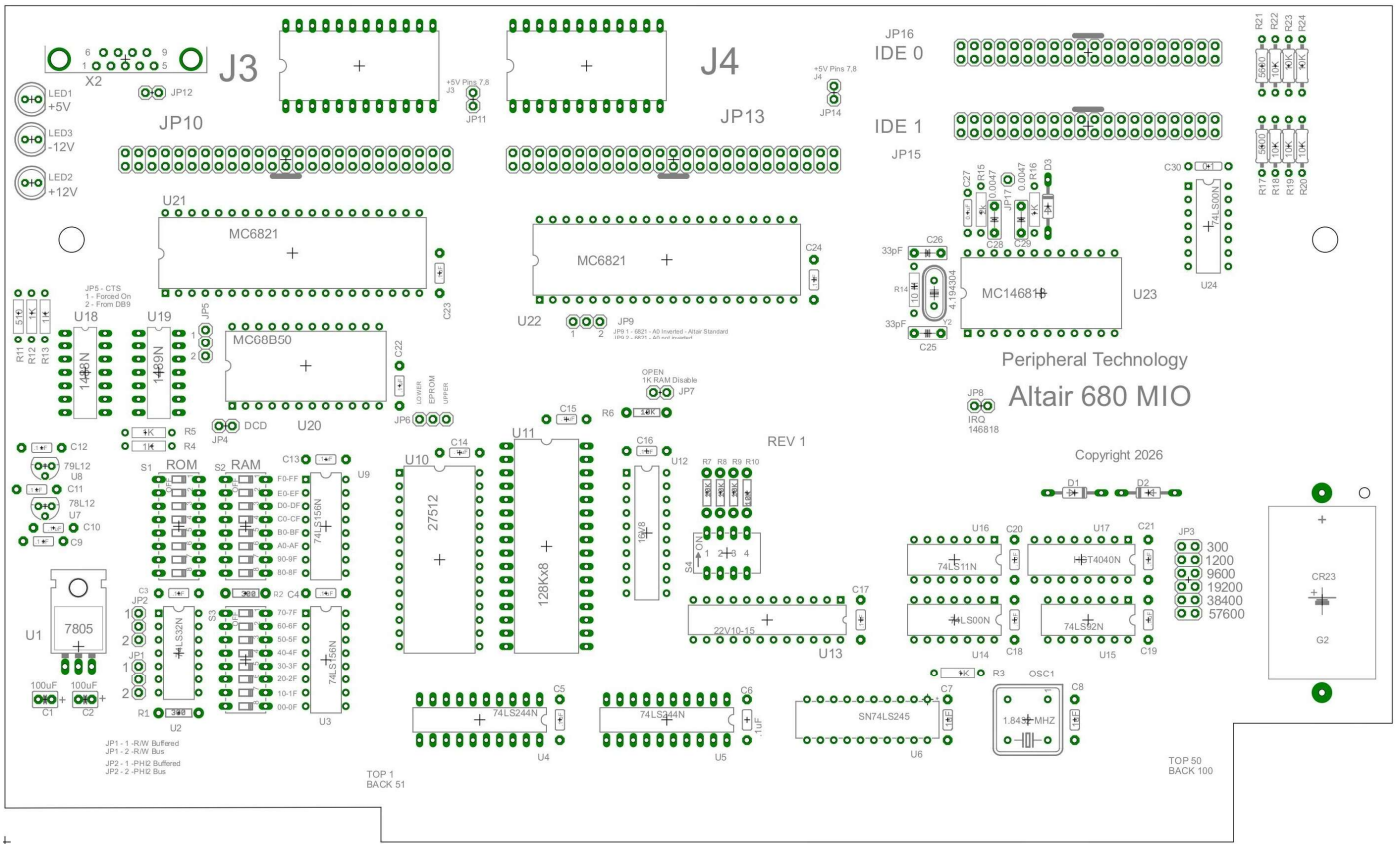
Switch S4 sets the starting address of the MIO board. Only one MIO board can be installed, but the MIO can be used with other MITS boards. The address of the RTC and IDE are not changed by S4. S4 only sets the addresses of the parallel and serial ports.

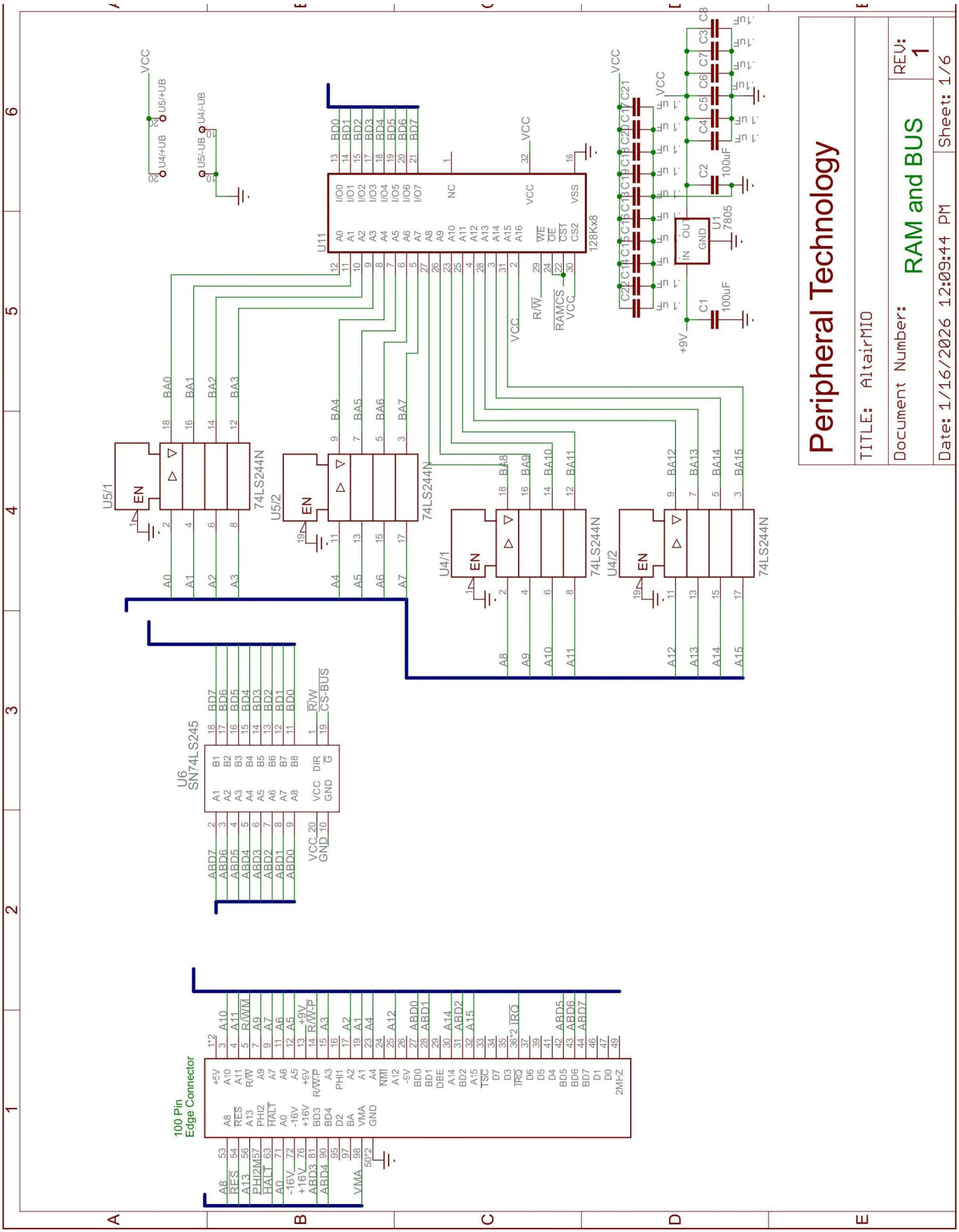
1	2	3	4	
ON	ON	ON	ON	F006-F00F
ON	ON	ON	OFF	F016-F01F
ON	ON	OFF	ON	F026-F02F
ON	ON	Off	OFF	F036-F03F
ON	OFF	ON	ON	F046-F04F
ON	OFF	ON	OFF	F056-F05F
ON	OFF	OFF	ON	F066-F06F
ON	OFF	OFF	OFF	F076-F07F
OFF	ON	ON	ON	F086-F08F
OFF	ON	ON	OFF	F096-F09F
OFF	ON	OFF	ON	F0A6-F0AF
OFF	ON	OFF	OFF	F0B6-F0BF

Other switch settings should not be used. The other switch positions would conflict with the RTC, IDE, or restart vectors.

680 MIO PARTS LIST

QUANTITY	DESIGNATION	DESCRIPTION
1	U1	DC-DC CONVERTER – RBT10W24S05 – DO NOT USE A 7805
1	U2	74LS32
2	U3,U9	74LS156
2	U4,U5	74LS244
1	U6	74LS245
1	U7	78L12
1	U8	79L12
1	U10	27C512
1	U11	128KX8 HM628128 STATIC RAM
1	U12	ATF16V8B-15PU
1	U13	ATF22V10C-15PU
2	U14,U24	74LS00
1	U15	74LS92
1	U16	74LS11
1	U17	CD4040
1	U18	1488
1	U19	1489
1	U20	MC6850P
2	U21,U22	MC6821P
1	U23	MC146818P
2	D1,D2	BAT42
1	D3	1N4148
1	OSC	1.8432 MHZ ½ SIZE OSCILLATOR
1	Y2	4.1943 MHZ CRYSTAL
3	LED1-LED3	GENERIC T-1-3/4 LED – ANY COLOR
2	R1-R2	300 OHM 1/4 WATT
6	R3-R5,R12-R13,R16	1K OHM
11	R6-R10,R18-R20 R22-24	10K
1	R11	470
1	R14	10M
1	R15	2K
2	R17,R21	5.6K
2	C1,C2	100UF 25V
	C3-C27,C30	0.1UF 25V
2	C25,C26	33PF
2	C28-C29	0.0047UF
3	S1-S3	8 POSITION DIP SWITCH
1	S4	4 POSITION DIP SWITCH
1		6X2 HEADER STRIP
5		3X1 HEADER STRIP
6		2X1 HEADER STRIP
2		40X2 SHROUDED HEADER KEYED
2		50X2 SHROUDED HEADER KEYED
1		BATTERY HOLDER
12		SHORTING SHUNTS
1		DB9F CONNECTOR
7		14 PIN IC SOCKETS
3		16 PIN IC SOCKET
4		20 PIN IC SOCKET
1		24 PIN IC SOCKET .3” WIDTH
4		24 PIN IC SOCKET .6” WIDTH
1		28 PIN IC SOCKET .6” WIDTH
1		32 PIN IC SOCKET
2		40 PIN IS SOCKET


Altair 680 MIO
Peripheral Technology
REV 1
Copyright 2026
J3
J4
IDE 0
IDE 1
JP10
JP13
JP15
JP16
MC6821
MC68B50
MC14681B
ROM
RAM
27512
128Kx8
7805
74LS244N
74LS245
74LS156N
74LS32N
74LS00N
74LS11N
74LS04N
74LS02N
SN74LS245
22V10-15
1.8432MHZ
4.194304
OPEN
1K RAM Disable
JP7
IRQ
146818
TOP 1
BACK 51
TOP 50
BACK 100
300
1200
9600
19200
38400
57600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RAM and BUS
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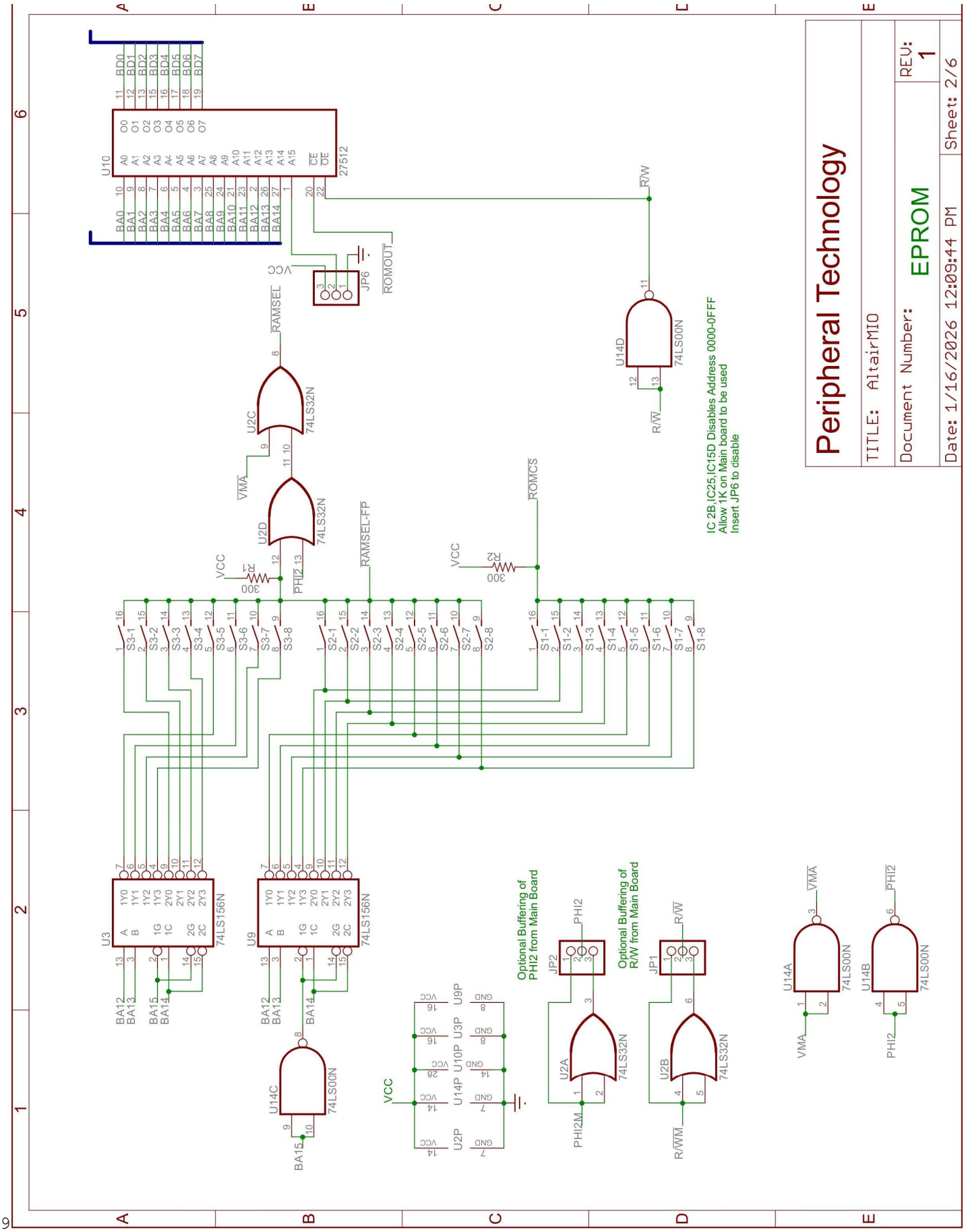
Sheet: 1/6
100 Pin Edge Connector
74LS244N
74LS245
SN74LS245
128Kx8
7805
100uF
VCC
+9V
R/W
CS-BUS
RAMCS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Document Number: EPROM
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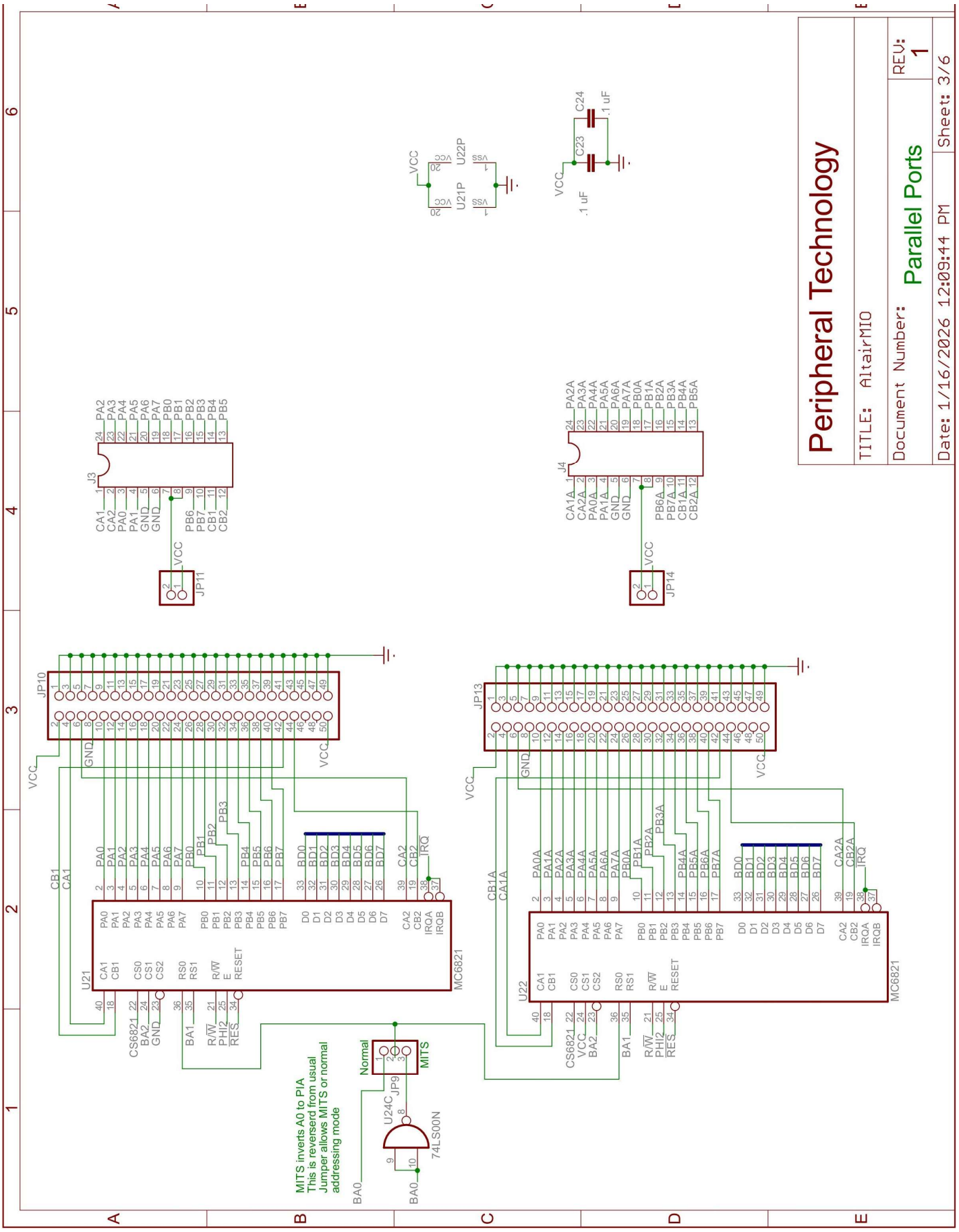
Sheet: 2/6
IC 2B,IC25,IC15D Disables Address 0000-0FFF
Allow 1K on Main board to be used
Insert JP6 to disable
Optional Buffering of PHI2 from Main Board
Optional Buffering of R/W from Main Board
U10
27512
U3
U9
74LS156N
U2C
U2D
74LS32N
U14C
U14D
74LS00N
U2A
U2B
U14A
U14B
JP1
JP2
JP6
RAMSEL
RAMSEL-FF
ROMCS
ROMOUT
VMA
PHI2
R/W
VCC


Peripheral Technology
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Document Number: Parallel Ports
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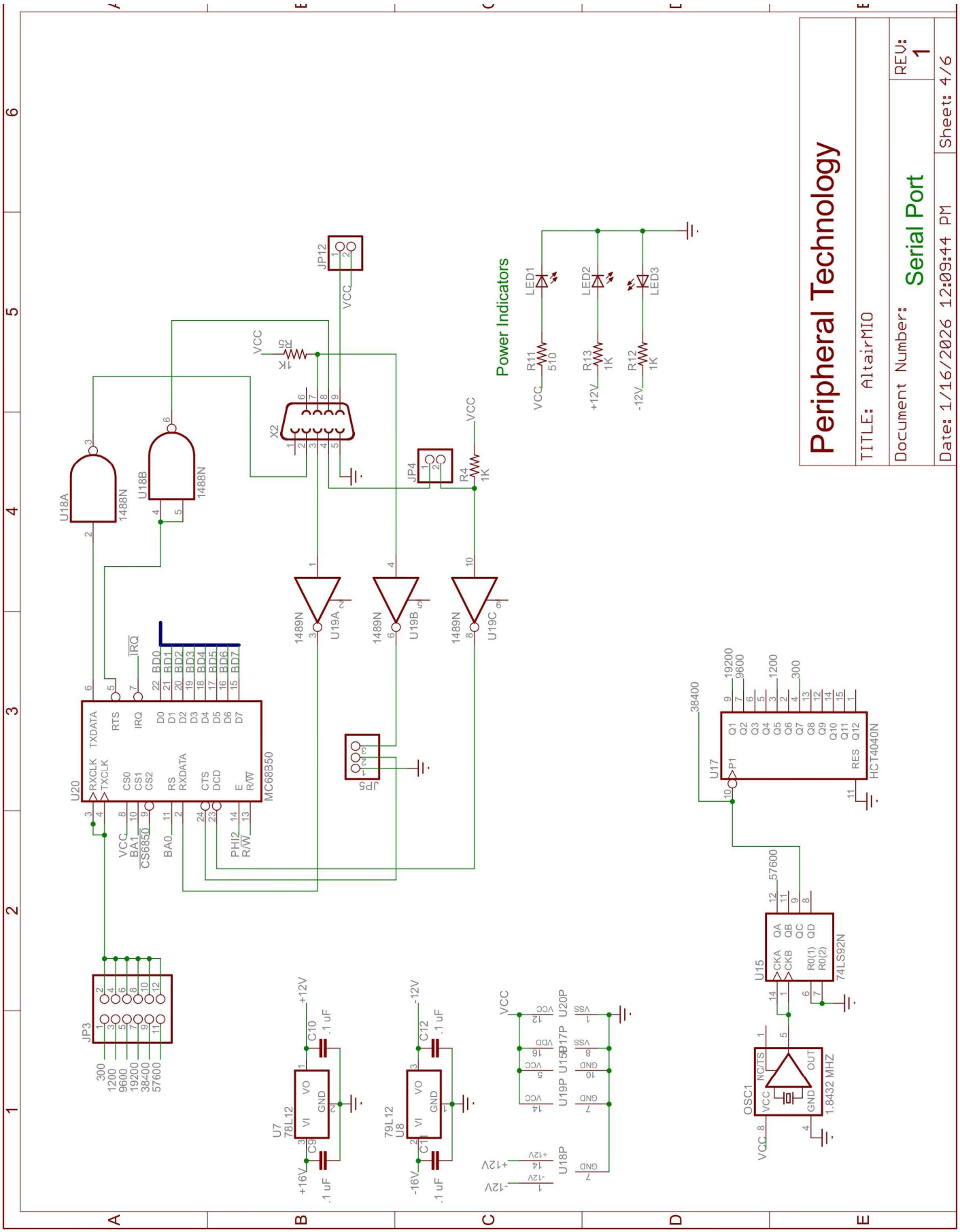
Sheet: 3/6
MITS inverts A0 to PIA
This is reverserd from usual
Jumper allows MITS or normal
addressing mode
Normal
MITS
74LS00N
MC6821
U21
U22
JP10
JP13
J3
J4
JP11
JP14
U21P
U22P
C23
C24
.1 uF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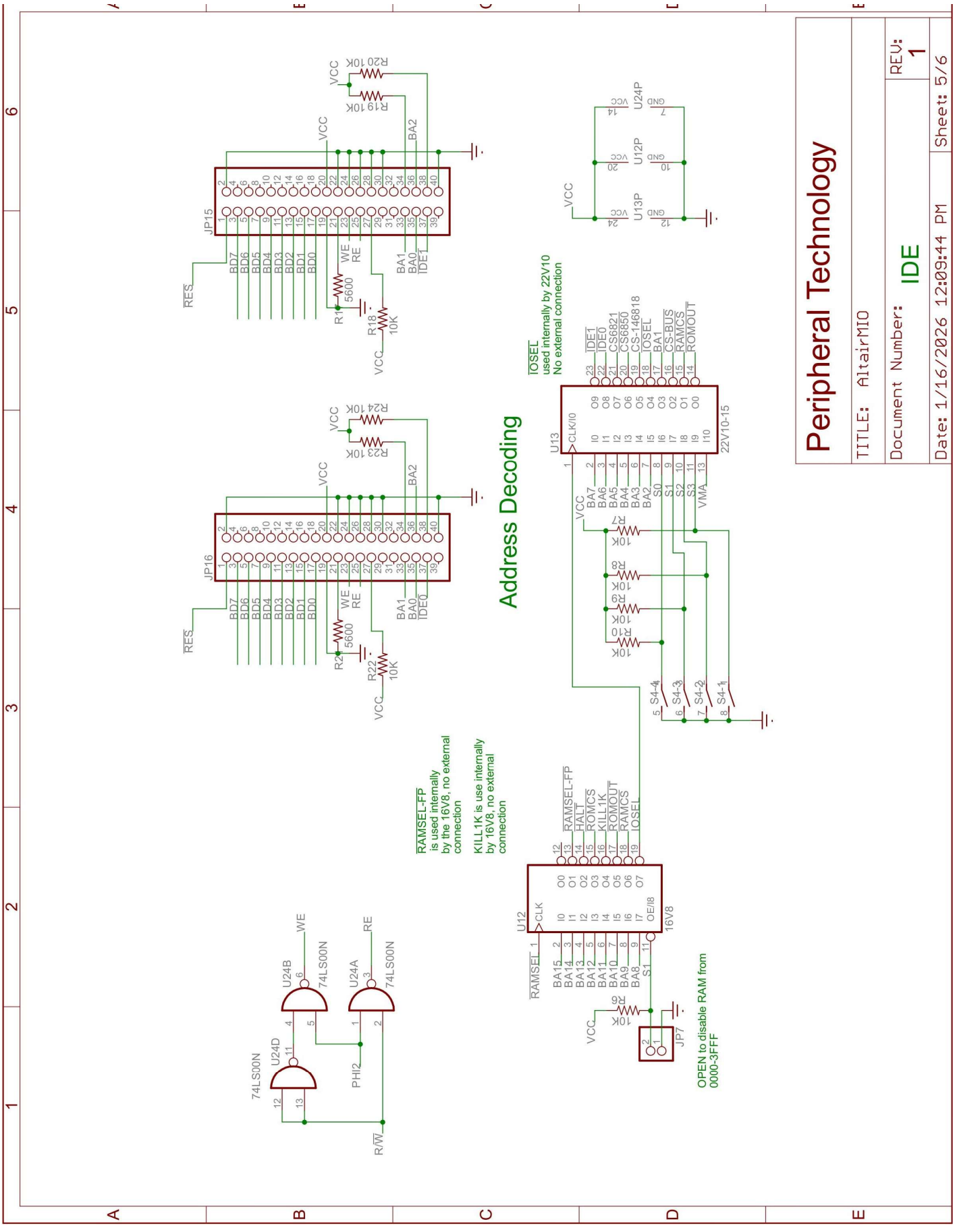
Sheet: 4/6
Power Indicators
LED1
LED2
LED3
R11 510
R13 1K
R12 1K
R4 1K
U18A 1488N
U18B 1488N
U19A 1489N
U19B 1489N
U19C 1489N
U20 MC68B50
U17 HCT4040N
U15 74LS92N
U7 78L12
U8 79L12
OSC1 1.8432 MHZ
JP3
JP4
JP12
X2
38400
57600
19200
9600
1200
300


Peripheral Technology
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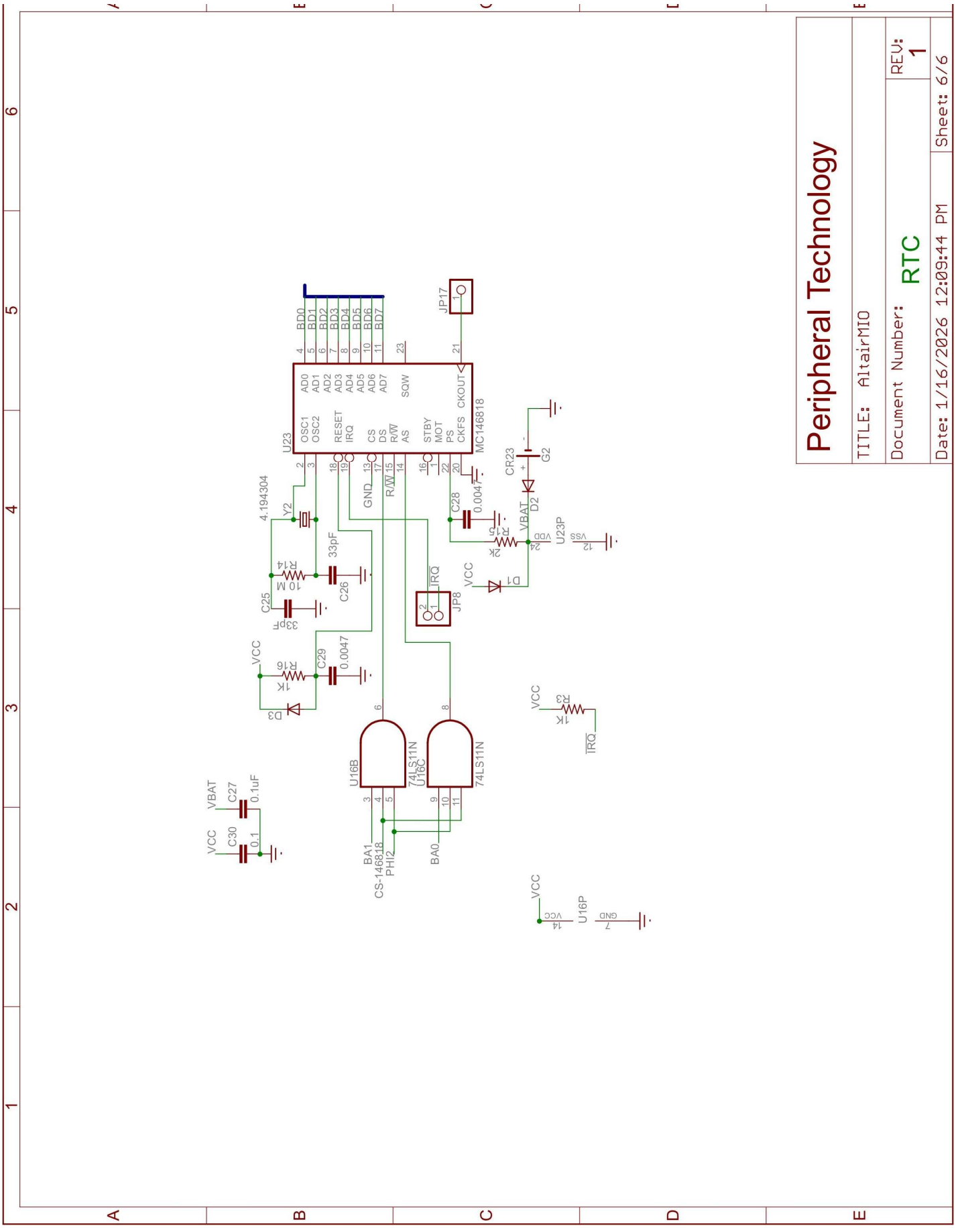
Sheet: 5/6
Address Decoding
IOSEL
used internally by 22V10
No external connection
RAMSEL-FP
is used internally
by the 16V8, no external
connection
KILL1K is use internally
by 16V8, no external
connection
OPEN to disable RAM from
0000-3FFF
JP15
JP16
JP7
U12
U13
U24B
U24A
U24D
74LS00N
16V8
22V10-15
RES
PHI2
R/W
WE
RE
VCC
S4-1
S4-2
S4-3
S4-4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Document Number: RTC
REV: 1
Date: 1/16/2026 12:09:44 PM
Sheet: 6/6
U23
MC146818
JP17
JP8
U16B
U16C
74LS11N
U16P
CR23
G2
D1
D2
D3
Y2
4.194304
33pF
C25
C26
C27
0.1uF
C28
0.0047
C29
0.0047
C30
0.1
R14
10 M
R15
2K
R16
1K
R3
1K
VCC
VBAT
GND
IRQ
BA0
BA1
PHI2
CS-146818

APPENDIX

Assembly Notes:

When sourcing parts do not use a 7805 for a voltage regulator. The Altair provides an extremely high voltage of nearly 10 volts. This can potentially overheat and reduce the life of the regulator. You should use a DC-DC convertor. A part number for one example is given in the parts list. The DC-DC regulator typically runs 10-20 degrees F above ambient temperature. A 7805 can run near 100C. A one AMP regulator is sufficient. The part number listed in the parts list can be obtained from Digikey.

A binary copy of the SWTBUG EPROM can be downloaded from the Peripheral Technology website. The binary is 8K in size. Be sure to locate this image at either 6000-7FFF or E000-FFFF in your 27C512 and set the appropriate upper/lower jumper – JP6.

PAL .JED files can be downloaded for U12 and U13. It is recommended to use an ATMEL brand GAL of the speed listed in the parts list. Other brands and speeds have not been tested and may not work properly. Don't potentially waste many hours troubleshooting a board because you substituted a different brand of GAL or a different speed. The Atmel part is typically in stock at Mouser or Digikey,

Buffered vs Unbuffered PHI2, R/W

The Unbuffered PHI2 and R/W signals are those from the Altair 680 main board. When selected by JP1 and JP2, the main board PHI2 and R/W are used by the MIO board. When the buffered selection is made, PHI2 and R/W are buffered by gates of a 74LS32 chip before being fed the MIO board. The PHI2 signal from the main board can vary depending on the modifications and chips used. The original design used a CD4050 to provide R/W and PHI2 to the expansion connector. The use of a CD4050 added approximately 100ns of delay, and the signals had a slow rise and fall times. A popular modification to the main board was to bypass the CD4050 and feed PHI2 directly to the expansion connector. While this appears to work in most systems you end up with PHI2 from the main board potentially driving a large number of chips. A better solution than bypassing the CD4050 is to use a 74HC4050. The Peripheral Technology Reproduction of the Altair 680 main board specs the use of a 74HC4050 instead of a CD4050. In testing of various Altair systems, some reproduction and some real Altairs with CD4050, 74HC4050, or the CD4050 bypassed it was found that some of the combinations didn't work if R/W and PHI2 was buffered in the prototype MIO board. For this reason, the REV1 version of the board has jumpers to select buffered vs unbuffered to feed the MIO. Early testing of the REV1 board seems to show buffered and unbuffered R/W and PHI2 work with all combinations of hardware. The suggestion is to configure the MIO for buffered. If you are having problems switch to unbuffered R/W and PHI2. You will know very quickly if your system is having problems. On the REV 0 board it was apparent very quickly if there was a problem. FLEX wouldn't boot and/or run for more than a minute or two. The memory in SWTBUG would also fail very quickly.

Address Map of 6850 and 6821s

The MIO board keeps the address map of the MC6850 and the MC6821s the same as the MITS UIO board. In most cases the MIO board should be able to replace a UIO board. The base address of the MC6850 and MC6821s can be set the same as the UIO board. MITS provided the ability to place the base address on 16 byte boundaries starting at address F000. The first 6 bytes in the 16 byte block were not used since these addresses were used by the main board.

xx06-xx07 – MC6850
xx08-xx0B – MC6821 J4 or JP13
xx0C-xx0F – MC6821 J3 or JP10

The organization of the MC6821 registers depends on jumper JP9. MITS elected to invert A0 to the MC6821. This reversed the data and status registers. JP9 allows use of an inverted A0 like MITS or a noninverted A0. If you have no need to be compatible with the MITS standard you can select a noninverted A0. Be aware that the Corsham SD boot and utilities in SWTBUG were setup to support the MITS standard of an inverted A0.

PAL EQUATIONS

PAL equations are provided should you wish to modify the PAL code. If you want to replace a damaged GAL you can download .jed files to program a GAL. It is not necessary to compile this source.

U12

```
Name     Altair 680 MIO decoding ;
PartNo   U12 ;
Date     11/07/25 ;
Revision 0 ;
Designer Frederic Brown ;
Company  Peripheral Technology ;
Assembly None ;
Location None ;
Device   g16v8a ;

/* *************** INPUT PINS *********************/

PIN 1   =  RAMIN                 ; /*  RAMCS From Switches qualified with PHI2 & VMA  */
PIN 2   =  A15                   ; /*                                                 */
PIN 3   =  A14                   ; /*                                                 */
PIN 4   =  A13                   ; /*                                                 */
PIN 5   =  A12                   ; /*                                                 */
PIN 6   =  A11                   ; /*                                                 */
PIN 7   =  A10                   ; /*                                                 */
PIN 8   =  A9                    ; /*                                                 */
PIN 9   =  A8                    ; /*                                                 */
PIN 11  =  S1                    ; /* Short to disable 1K at 0000     */
PIN 13  =  RAMIN1                ; /* RAMCS not qualified with PHI2,VMA. Needed for front panel */
PIN 14  =  HALT                  ; /* HALT from Bus - Active Low      */
PIN 15  =  ROMIN                 ; /* ROMCS from switches             */



/* *************** OUTPUT PINS *********************/

PIN 16  =  KILL1K           ; /*  Decode for memory 0000-03FF         */
PIN 17  =  ROMOUT           ; /*  Removes addresses F000-F0FF from EPROM access */
PIN 18  =  RAMOUT           ; /*  RAMCS with 1K killed if switch set  */
PIN 19  =  IOSEL            ; /*  Address decode F000-F0FF            */


/** Logic Equations **/

/* Address Select for F000-F0FF */

!IOSEL  =   A15 & A14 & A13 & A12 & !A11 & !A10 & !A9 & !A8 ;

/* Allow EPROM in MIO to replace 1702s in Main Board. Since 4K
   blocks are decoded, memory from F000-F0FF must be disabled
   for Altair IO. This changes the top EPROM 4K block from
   F000-FFFF to F100-FFFF                                  */

 ROMOUT = ROMIN # ( A15 & A14 & A13 & A12 & !A11 & !A10 & !A9 & !A8 ) ;


/* Kill external RAM from 0000-03FF to allow 1K RAM on Altair main board to
   be used.  This eliminates the need to modify the Main Board to deactivate
   the 1K of RAM typically at Address 0000-03FF */

/* This equation was too complex for the GAL so it was rewritten to use 2 outputs

    RAMOUT = (RAMIN & !( !A15 & !A14 & !A13 & !A12 & !A11 & !A10  & S1  ))
              & (RAMIN1 & HALT ) ;  */

KILL1K =  !A15 & !A14 & !A13 & !A12 & !A11 & !A10  & S1 & !RAMIN1 ;  /* Decode for the Main board 1K RAM */

RAMOUT = (RAMIN # KILL1K)     /* RAMIN - Ram select qualified with VMA and PHI2 */
  &  ( RAMIN1 # KILL1K # HALT ) ;      /* RAMIN1 - RAM select not qualified with VMA,PHI2 */
                               /* Without using RAMIN1 the front panel LEDs don't work */
```

U13

```
Name     Altair 680 MIO decoding ;
PartNo   U13 ;
Date     10/26/25 ;
Revision 0 ;
Designer Frederic Brown ;
Company  Peripheral Technology ;
Assembly None ;
Location None ;
Device   p22v10 ;

/* *************** INPUT PINS *********************/

PIN 1   =  FFSEL                 ; /*  Address F0xx decode           */
PIN 2   =  A7                    ; /*                                */
PIN 3   =  A6                    ; /*                                */
PIN 4   =  A5                    ; /*                                */
PIN 5   =  A4                    ; /*                                */
PIN 6   =  A3                    ; /*                                */
PIN 7   =  A2                    ; /*                                */
PIN 8   =  S0                    ; /* Select 1 of 16 Address blocks  */
PIN 9   =  S1                    ; /*                                */
PIN 10  =  S2                    ; /*                                */
PIN 11  =  S3                    ; /*                                */
PIN 13  =  VMA                   ; /*                                */
PIN 14  =  ROMCS                 ; /*  Rom Decode                    */
PIN 15  =  RAMCS                 ; /*  RAM Decode                    */
PIN 17  =  A1                    ; /*                                */

/* *************** OUTPUT PINS *********************/

PIN 16  =  CSBUS            ; /*  Chip enable bus driver            */
PIN 18  =  IOSEL            ; /*  Decode for board address          */
PIN 19  =  CS146818         ; /*  146818 F0C0-F0CF                  */
PIN 20 =   CS6850           ; /*  6850 - F0x6 and F0x7              */
PIN 21  =  CS6821           ; /*  6821 F0xy  Decode for Both 6821s  */
PIN 22  =  IDE0             ; /*  IDE0 - F0D0-F0DF                  */
PIN 23  =  IDE1             ; /*  IDE1 - F0E0-F0EF                  */


/** Logic Equations **/

/* Enable the data buffer when anything on the board is accessed */

/* CSBUS  =   ROMCS & RAMCS & CS146818 & CS6821 & CS6850 & IDE0 & IDE1 ; */

CSBUS  =   ROMCS & RAMCS & !CS146818 & CS6850 & !CS6821 & IDE0 & IDE1 ;

/* Use switch bits S0 to S3 to match bits A7 to A3.  This will set the basic board address for the
   2 6821 and 6850 chip.  Altair placed the board on 16 bit boundary from FF00 to FFF0. Only bits 06-FF
   are used. 06-07 = 6850, 08-0B = First 6821 and 0C-0F = Second 6821.  Bits 00-05 are not used since they
   would conflict with the 6850 at FF00-FF01 and the configuration register at FF02 should the board be
   configured for F000-FF0F. The board can start at these addresses
   F000, F010, F020, F030, F040, F050, F060, F070, F080, F090, F0A0, F0B0
   These addresses cannot be used since they would conflict with MIO IO - F0C0, F0D0, F0E0
   The last address FFF0 should not be selected since it would conflict with the 6800 restart vectors. */

IOSEL =  (A7 $! S3) & (A6 $! S2) & (A5 $! S1) & (A4 $! S0) ;

!IDE0  = !FFSEL & A7 & A6 & !A5 & A4 & VMA ;                  /*  F0D0-F0DF */

!IDE1  =  !FFSEL &  A7 &  A6 & A5 & !A4 & VMA ;               /*  F0E0-F0EF */

CS6821 = !FFSEL & IOSEL & A3 ;    /* Address F000 + switch selected address */

!CS6850 = !FFSEL & IOSEL & !A3 & A2 & A1 ;  /* Address = F0x6 to FFx7 - x=switch address */

CS146818 = !FFSEL & A7 & A6 & !A5 & !A4 & VMA ; /* F0C0 - F0CF */
```

Serial DB9F Pinouts

The DB9F connector works with common USB to DB9M cables. There are many brands of these cables, and they are sold by many online sellers. One brand is OIKWAN AQ-17. OIKWAN is sold by AMAZON US.

Pin		
2	TxD	Transmit Data from 6850
3	RXD	Received Data to 6850
4	DCD	Input to 6850 – Enabled by JP4
5	GND	
7	CTS	Input 6850 – Controlled by JP5
8	RTS	Output from 6850
9	+5V	Enabled by JP12

The option of +5V on Pin 9 is intended to power a serial drive server such as the “ESP32 FDC+ SERIAL DRIVE SERVER” available from Deltec Enterprises. With a custom RS232 cable this eliminates the need to find a power source for a small external device.

CTS – CTS can be fed from the DB9-Pin 7 or forced on by jumper JP5. Position 1 of JP5 forces CTS on. Position 2 feeds Pin 9 through a 1489 to the CTS input of the 6850.

DCD – To use DCD short JP4. If JP4 is not shorted DCD is always forced on to the 6850.