Corsham Technologies, LLC
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SS-50 Prototyping Board

Introduction

Thank you for buying our SS-50 Prototyping Board! We hope you build some really cool projects on it!

Features

During the course of developing most of our SS-50 boards, we constantly realized it would have been much easier and less expensive to lay out a new design on a prototyping board. So here it is!

Features include:

- Access to all SS-50/SS-50C bus signals.
- Buffering of most signals.
- Buffers can be disabled and driven in either direction.
- Ability to build either slave or master devices
- Reasonably large prototyping area using solderless jumper board.
- 10 pin connector for expansion to external devices/boards.

Signal Locations

Any signal name starting with "/" is active low or inverted.

Signal names are the same for SS-50 and SS-50C unless there is an "or" between signal names, in which case the first name is for SS-50 and the second is for SS-50C.

JP1

Pin	Signal
1	A14
2	A15
3	/D7
4	/D6
5	/D5
6	/D4
7	/D3
8	/D2
9	/D1
10	/D0

JP2

Pin	Signal
1	A4
2	A5
3	A6
4	A7
5	A8
6	A9
7	A10
8	A11
9	A12
10	A13

JP3

Pin	Signal
1	+8 VDC
2	+8 VDC
3	+8 VDC
4	Ground
5	Ground
6	Ground
7	A0
8	A1
9	A2
10	A3

JP4

Pin	Signal
1	/VMA
2	/PHASE 2 or /E
3	UD 2 or /Q
4	UD 1 or /FIRQ
5	/IRQ
6	/NMI
7	/M_RST
8	Unused
9	+12 VDC
10	-12 VDC

JP5

Pin	Signal
1	B1200 or A16
2	B600 or A17
3	B300 or A18
4	B150 or A19
5	B110 or /BUSRQ
6	/HALT
7	/PHASE 1
8	BA
9	/RESET
10	R/W

JP6

Pin	Signal
1	/DATA_ENABLE
2	DATA_DIR
3	/ADDR_ENABLE
4	ADDR_DIR
5	/MISC_ENABLE
6	MISC_DIR
7	7, 8, 9, 10 shorted
8	
9	
10	

Buffering

JP6 has access to three sets of control lines, each set having a /ENABLE and a DIR line. They provide complete control of the buffers, allowing the prototyping board to be used for a bus slave, such as a memory, I/O or video board, or as a master such as a CPU board.

By default, all of the /ENABLE lines are pulled low via pull-down resistors, which results in the buffers being active so that signals on the SS-50 bus are visible.

By default, all of the DIR lines are pulled so that the prototyping board receives all signals but does not drive the bus. For slave devices, it is likely that only the DATA_DIR line is pulled low to write onto the data lines on the SS-50 bus. For master boards, the address and control lines are probably driven as well.

Why This?

Back when SWTPC was around, I was a teenager without much money to spare. I got their catalogs and was intrigued by their inexpensive kits and simple designs that could be assembled by average people. The entry point for a working system was a bit beyond my means, so I ended up with a KIM-1 instead.

Years later, I have my own company that has been making Apple/Franklin and KIM-1 expansion boards and one night I decided it was within my abilities to make a clone of the original SWTPC machine. By using some parts available now, the design can be simplified.

Bob Applegate
April 7th, 2019

Revision History

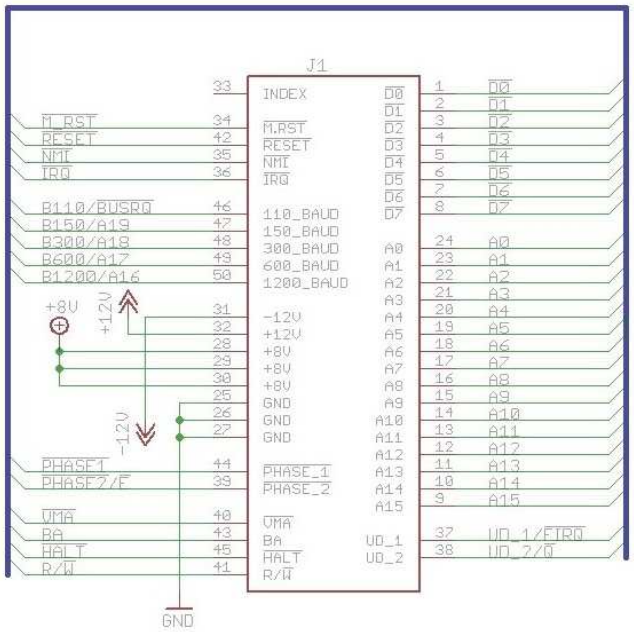
Version	Changes
1	Initial release 2018
2	Added signal names to silkscreen. Added array of plated through holes on right side of board.

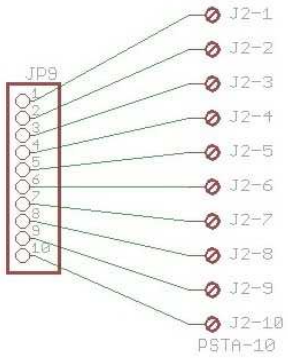
Errata

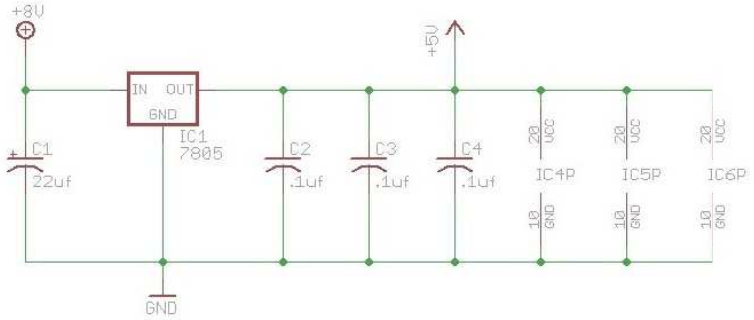
None

Parts List

Part	Number	Description
PCB	1	Printed Circuit Board (Corsham Tech)
J1	5	Molex 09-52-3101
J2	1	Terminal block, Digikey 277-1630-ND
C1	1	10 to 22uf, 25v electrolytic capacitor
C2-C4	3	.1 uf disc capacitor
IC1	1	7805 +5 VDC regulator, TO-220 case
IC3	1	74LS640
IC4-IC6	3	74LS245
	4	20 pin socket for IC3-IC6
R1-R6	6	6.8k ¼ watt resistor
JP1-JP9	9	1x10 SIP female header







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Corsham Tech, LLC
Bus connection, Power

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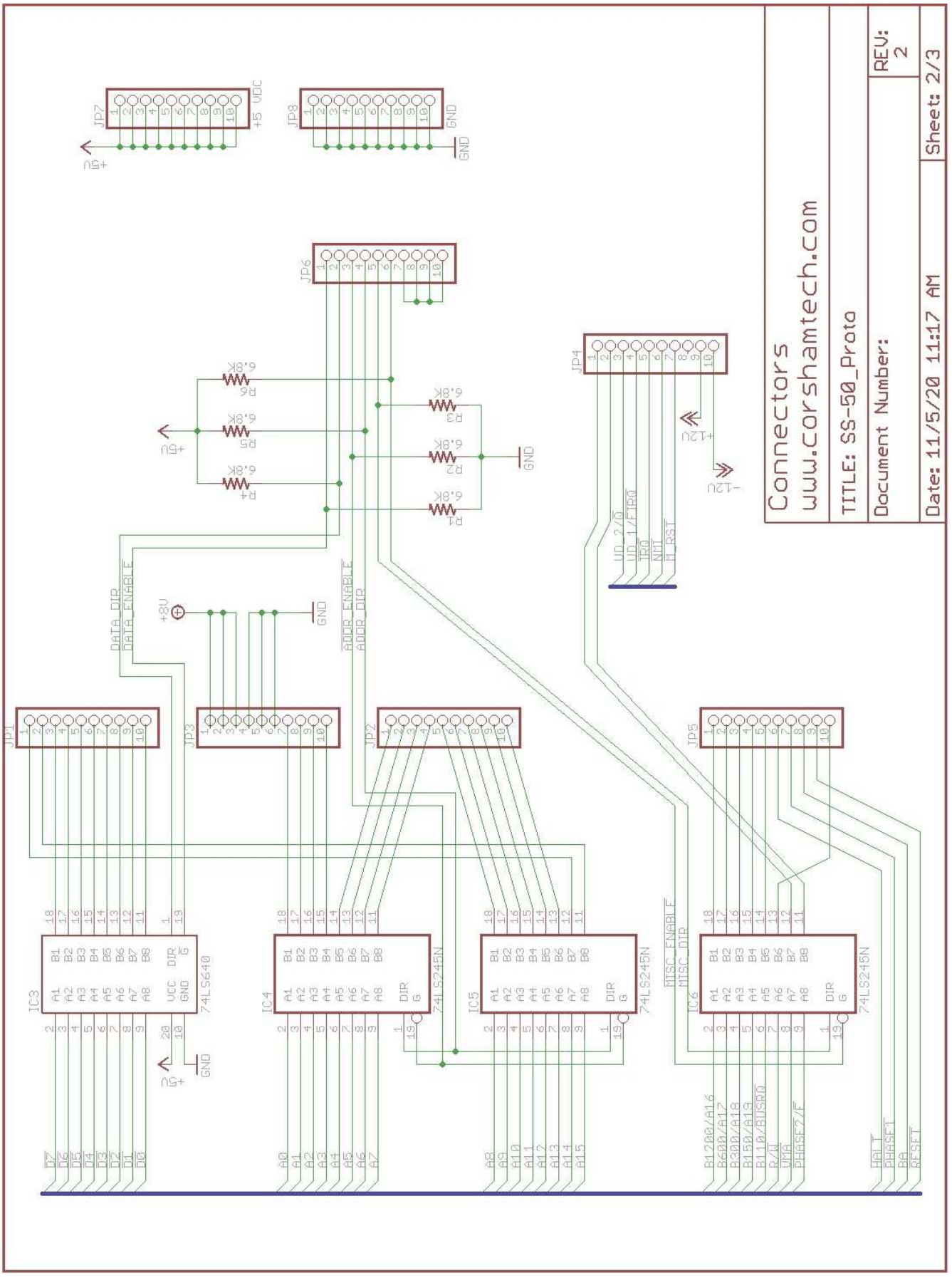
Connectors
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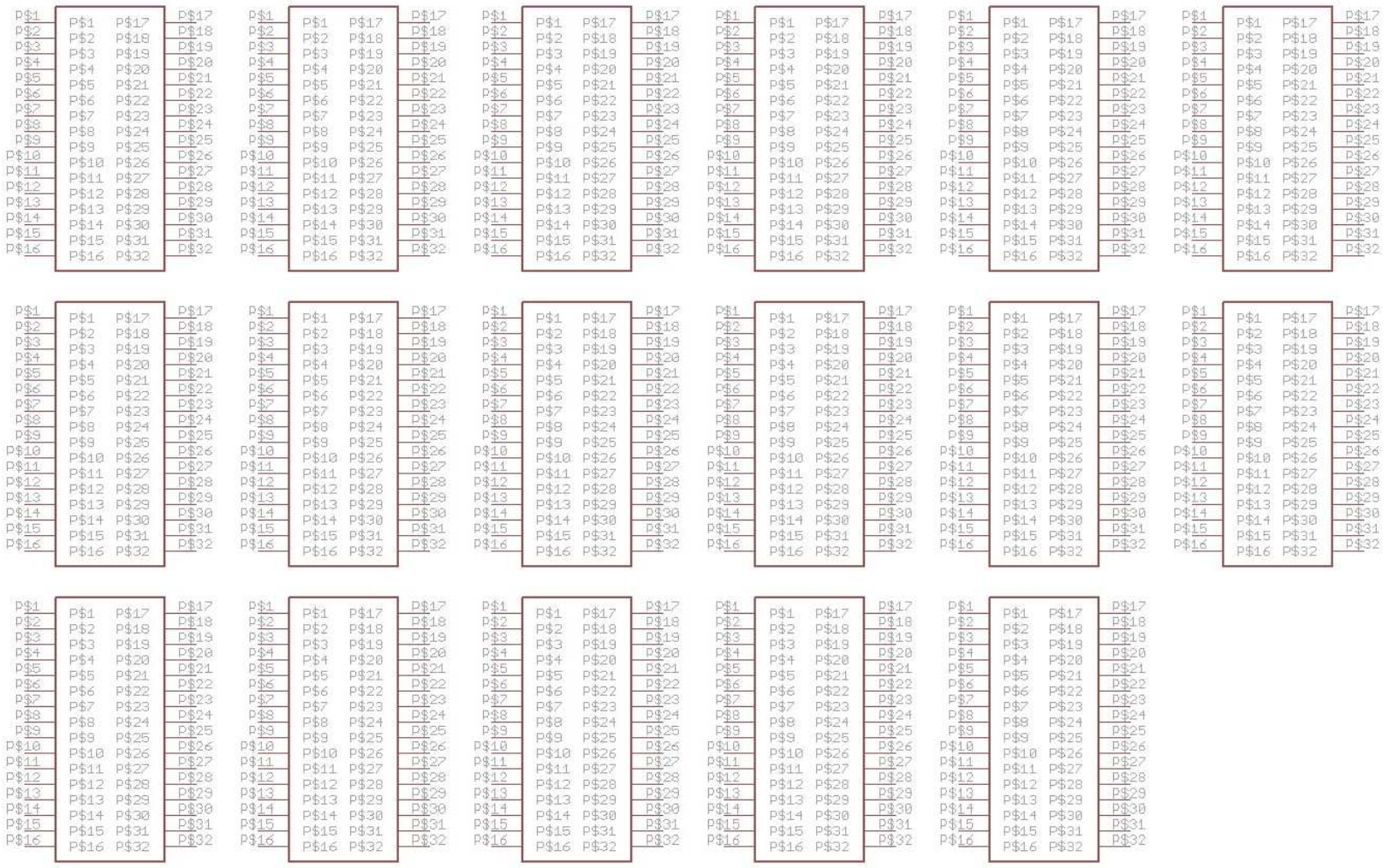
JP1
JP2
JP3
JP4
JP5
JP6
JP7
JP8
+5 VDC
GND
+5V
+12V
-12V
+8V
6.8K
DATA_DIR
DATA_ENABLE
ADDR_ENABLE
ADDR_DIR
MISC_ENABLE
MISC_DIR
IC3
IC4
IC5
IC6
74LS640
74LS245N
D7
D6
D5
D4
D3
D2
D1
D0
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
R/W
VMA
HALT
RESET



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